MC78LC00 Series

Micropower Voltage Regulator

The MC78LC00 series of fixed output low dropout linear regulators are designed for handheld communication equipment and portable battery powered applications which require low quiescent current. The MC78LC00 series features an ultra−low quiescent current of 1.1 μA. Each device contains a voltage reference unit, an error amplifier, a PMOS power transistor, and resistors for setting output voltage.

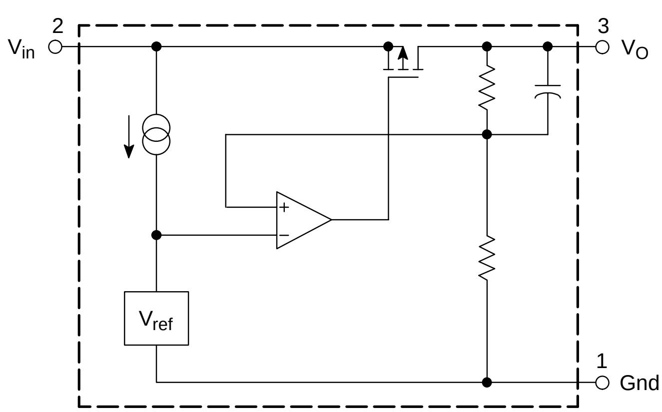
The MC78LC00 has been designed to be used with low cost ceramic capacitors and requires a minimum output capacitor of 0.1 μF. The device is housed in the micro−miniature Thin SOT23−5 surface mount package and SOT−89, 3 pin. Standard voltage versions are 1.5, 1.8, 2.5, 2.7, 2.8, 3.0, 3.3, 4.0, and 5.0 V. Other voltages are available in 100 mV steps.

Features

- Low Quiescent Current of 1.1 μA Typical
- Excellent Line and Load Regulation
- Maximum Operating Voltage of 12 V
- Low Output Voltage Option
- High Accuracy Output Voltage of 2.5%
- Industrial Temperature Range of −40°C to 85°C
- Two Surface Mount Packages (SOT−89, 3 Pin, or SOT−23, 5 Pin)
- Pb−Free Packages are Available

Typical Applications

- Battery Powered Instruments
- Hand−Held Instruments
- Camcorders and Cameras



This device contains 8 active transistors.

Figure 1. Representative Block Diagram

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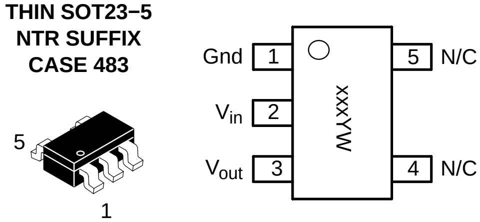
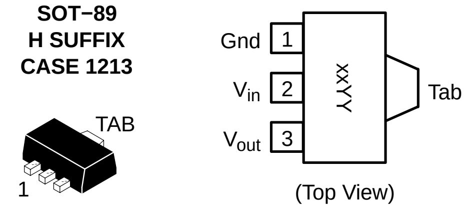
MARKING DIAGRAMS AND PIN CONNECTIONS

THIN SOT23−5
NTR SUFFIX
CASE 483



(Top View)

SOT−89
H SUFFIX
CASE 1213



(Top View)

(Tab is connected to Pin 2)

xxx = Version
Y = Year
W = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

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March, 2005 − Rev. 8

Publication Order Number:
MC78LC00/D

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	Gnd	Power supply ground
2	V_{in}	Positive power supply input voltage
3	V_{out}	Regulated Output
4	N/C	No Internal Connection
5	N/C	No Internal Connection

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	12	V
Output Voltage	V_{out}	−0.3 to V_{in} +0.3	V
Power Dissipation and Thermal Characteristics Case 483−01 (Thin SOT23−5) NTR Suffix Power Dissipation @ T_A = 85°C Thermal Resistance, Junction−to−Ambient Case 1213 (SOT−89) H Suffix Power Dissipation @ T_A = 25°C Thermal Resistance, Junction−to−Ambient	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 140 280 300 333	 mW °C/W mW °C/W
Operating Junction Temperature	T_J	+125	°C
Operating Ambient Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C
Lead Soldering Temperature @ 260°C	T_{solder}	10	sec

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS (V_{in} = $V_{out(nom.)}$ + 1.0 V, C_{in} = 1.0 μF, C_{out} = 1.0 μF, T_J = 25°C, unless otherwise noted.) (Note 5)

NTR SUFFIX

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_A = 25°C, I_{out} = 1.0 mA) 1.5 V 1.8 V 2.5 V 2.7 V 2.8 V 3.0 V 3.3 V 4.0 V 5.0 V	V_{out}	 1.455 1.746 2.425 2.646 2.744 2.94 3.234 3.9 4.90	 1.5 1.8 2.5 2.7 2.8 3.0 3.3 4.0 5.0	 1.545 1.854 2.575 2.754 2.856 3.06 3.366 4.1 5.10	V
Output Voltage (T_A = −40°C to 85°C) 1.5 V 1.8 V 2.5 V 2.7 V 2.8 V 3.0 V 3.3 V 4.0 V 5.0 V	V_{out}	 1.455 1.746 2.425 2.619 2.716 2.910 3.201 3.9 4.90	 1.5 1.8 2.5 2.7 2.8 3.0 3.3 4.0 5.0	 1.545 1.854 2.575 2.781 2.884 3.09 3.399 4.1 5.10	V
Line Regulation (V_{in} = $V_{O(nom.)}$ + 1.0 V to 12 V, I_{out} = 1.0 mA)	Reg_{line}	−	0.05	0.2	%/V
Load Regulation (I_{out} = 1.0 mA to 10 mA)	Reg_{load}	−	40	60	mV
Output Current (Note 6) 1.5 V, 1.8 V (V_{in} = 4.0 V) 2.5 V, 2.7 V, 2.8 V, 3.0 V (V_{in} = 5.0 V) 3.3 V (V_{in} = 6.0 V) 4.0 V (V_{in} = 7.0 V) 5.0 V (V_{in} = 8.0 V)	I_{out}	 35 50 50 80 80	 50 80 80 80 100	 − − − − −	mA
Dropout Voltage (I_{out} = 1.0 mA, Measured at V_{out} −3.0%) 1.5 V 1.6 V−3.2 V 3.3 V−3.9 V 4.0 V−5.0 V	V_{in}−V_{out}	 − − − −	 35 30 30 30	 70 60 53 38	mV
Quiescent Current (I_{out} = 1.0 mA to $I_{O(nom.)}$)	I_Q	−	1.1	3.6	μA
Output Voltage Temperature Coefficient	T_c	−	±100	−	ppm/°C
Output Noise Voltage (f = 1.0 kHz to 100 kHz)	V_n	−	89	−	μVrms

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per MIL−STD−883, Method 3015
   Machine Model Method 200 V
2. Latch up capability (85°C) ±100 mA
3. Maximum package power dissipation limits must be observed.
   $$PD = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$
4. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
5. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
6. Output Current is measured when V_{out} = V_{O1} − 3% where V_{O1} = V_{out} at I_{out} = 0 mA.

ELECTRICAL CHARACTERISTICS (V_{in} = $V_{out(nom.)}$ + 1.0 V, C_{in} = 1.0 μF, C_{out} = 1.0 μF, T_J = 25°C, unless otherwise noted.) (Note 11)

HT SUFFIX

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage					V
30HT1 Suffix (V_{in} = 5.0 V)		2.950	3.0	3.075	
33HT1 Suffix (V_{in} = 5.0 V)		3.218	3.3	3.382	
40HT1 Suffix (V_{in} = 6.0 V)		3.900	4.0	4.100	
50HT1 Suffix (V_{in} = 7.0 V)		4.875	5.0	5.125	
Line Regulation V_{in} = [V_O + 1.0] V to 10 V, I_O = 1.0 mA	Reg_{line}	−	0.05	0.2	%/V
Load Regulation (I_O = 1.0 to 10 mA)	Reg_{load}				mV
30HT1 Suffix (V_{in} = 5.0 V)		−	40	60	
33HT1 Suffix (V_{in} = 6.0 V)		−	40	60	
40HT1 Suffix (V_{in} = 7.0 V)		−	50	70	
50HT1 Suffix (V_{in} = 8.0 V)		−	60	90	
Output Current (Note 12)	I_O				mA
30HT1 Suffix (V_{in} = 5.0 V)		35	50	−	
33HT1 Suffix (V_{in} = 6.0 V)		35	50	−	
40HT1 Suffix (V_{in} = 7.0 V)		45	65	−	
50HT1 Suffix (V_{in} = 8.0 V)		55	80	−	
Dropout Voltage	$V_{in} - V_O$				mV
30HT1 Suffix (I_O = 1.0 mA)		−	40	60	
33HT1 Suffix (I_O = 1.0 mA)		−	35	53	
40HT1 Suffix (I_O = 1.0 mA)		−	25	38	
50HT1 Suffix (I_O = 1.0 mA)		−	25	38	
Quiescent Current	I_{CC}				μA
30HT1 Suffix (V_{in} = 5.0 V)		−	1.1	3.3	
33HT1 Suffix (V_{in} = 5.0 V)		−	1.1	3.3	
40HT1 Suffix (V_{in} = 6.0 V)		−	1.2	3.6	
50HT1 Suffix (V_{in} = 7.0 V)		−	1.3	3.9	
Output Voltage Temperature Coefficient	T_C	−	±100	−	ppm/°C

7. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per MIL−STD−883, Method 3015
   Machine Model Method 200 V
8. Latch up capability (85°C) ±100 mA
9. Maximum package power dissipation limits must be observed.

$$PD = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

10. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
11. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
12. Output Current is measured when $V_{out} = V_{O1} - 3\%$ where $V_{O1} = V_{out}$ at I_{out} = 0 mA.

DEFINITIONS

Load Regulation

The change in output voltage for a change in output current at a constant temperature.

Dropout Voltage

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 3% below its nominal. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

Maximum Power Dissipation

The maximum total dissipation for which the regulator will operate within its specifications.

Quiescent Current

The quiescent current is the current which flows through the ground when the LDO operates without a load on its output: internal IC operation, bias, etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse technique such that the average chip temperature is not significantly affected.

Line Transient Response

Typical over and undershoot response when input voltage is excited with a given slope.

Maximum Package Power Dissipation

The maximum power package dissipation is the power dissipation level at which the junction temperature reaches its maximum operating value, i.e. 125°C. Depending on the ambient power dissipation and thus the maximum available output current.

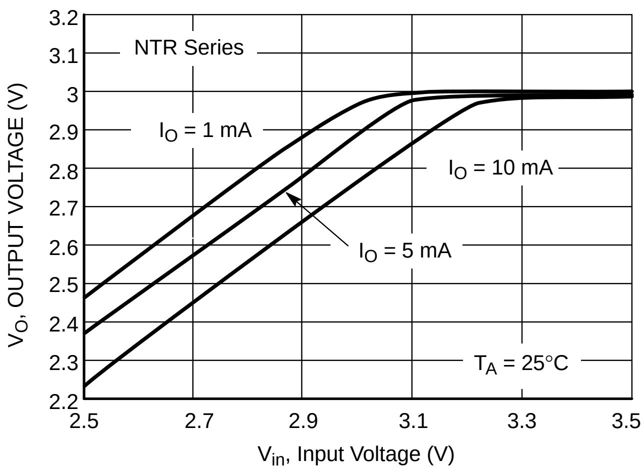


Figure 2. Output Voltage versus Input Voltage

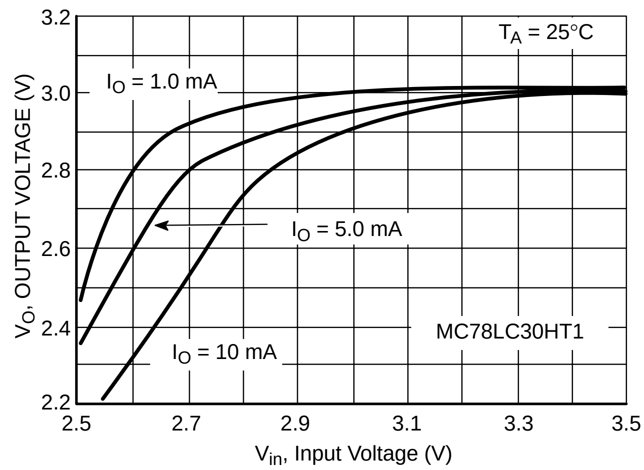


Figure 3. Output Voltage versus Input Voltage

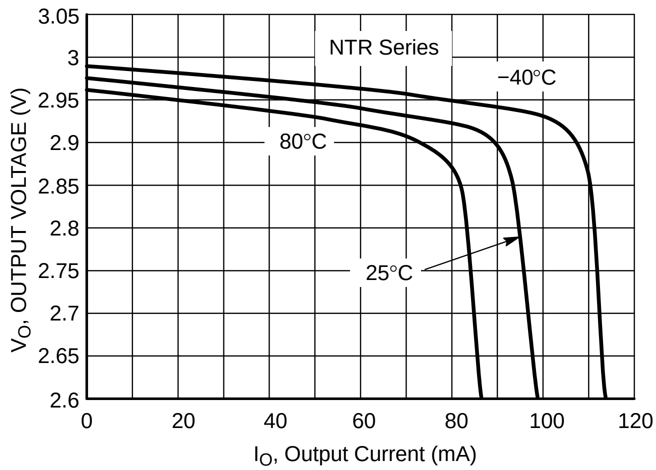


Figure 4. Output Voltage versus Output Current

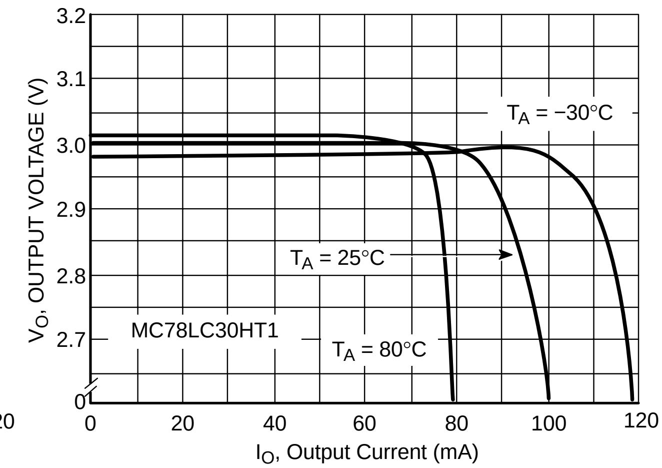


Figure 5. Output Voltage versus Output Current

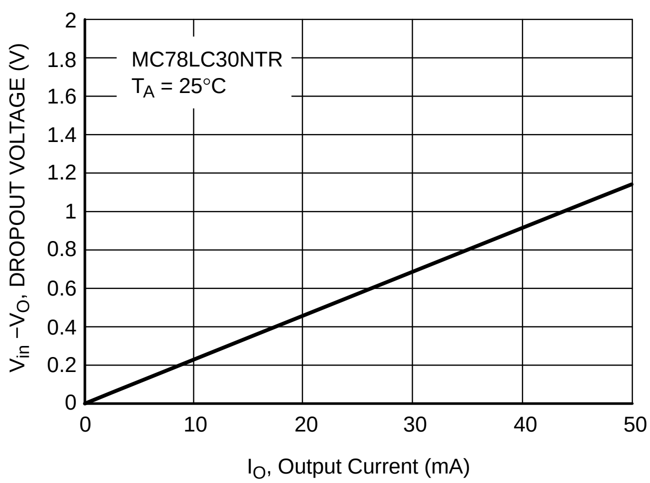


Figure 6. Dropout Voltage versus Output Current

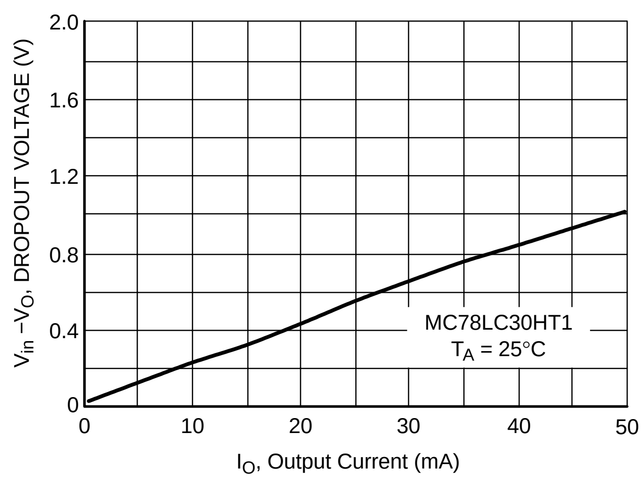


Figure 7. Dropout Voltage versus Output Current

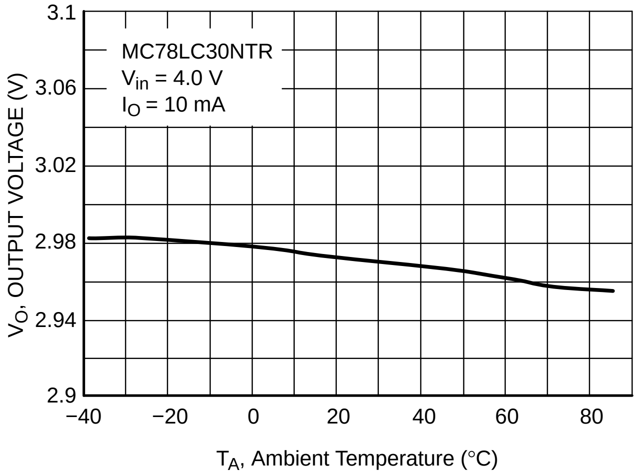


Figure 8. Output Voltage versus Temperature

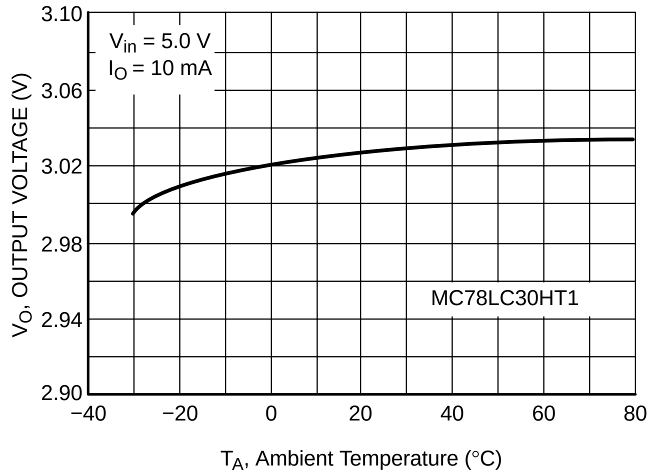


Figure 9. Output Voltage versus Temperature

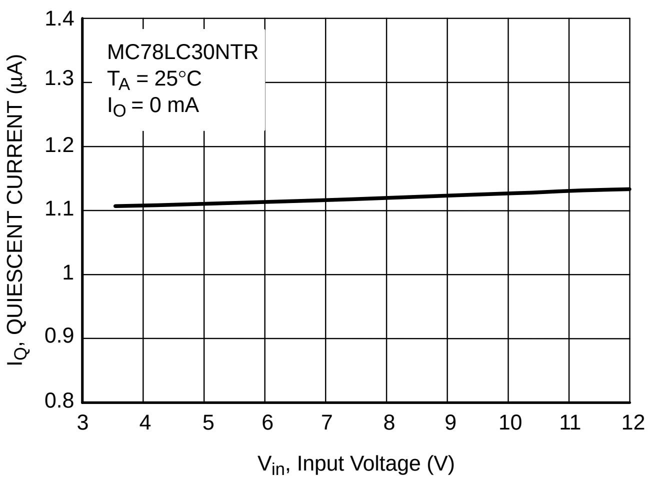


Figure 10. Quiescent Current versus Input Voltage

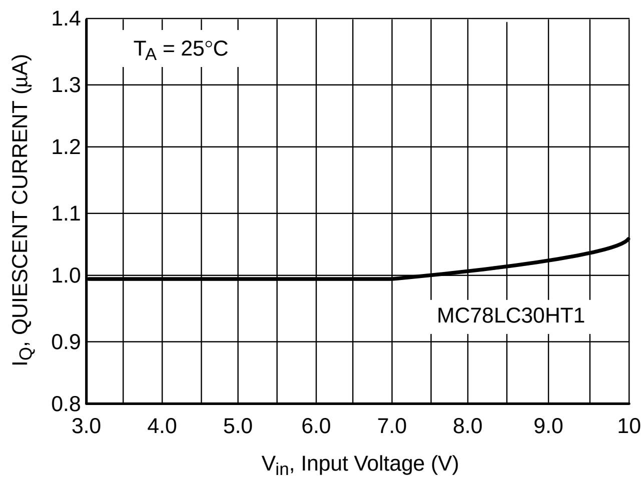


Figure 11. Quiescent Current versus Input Voltage

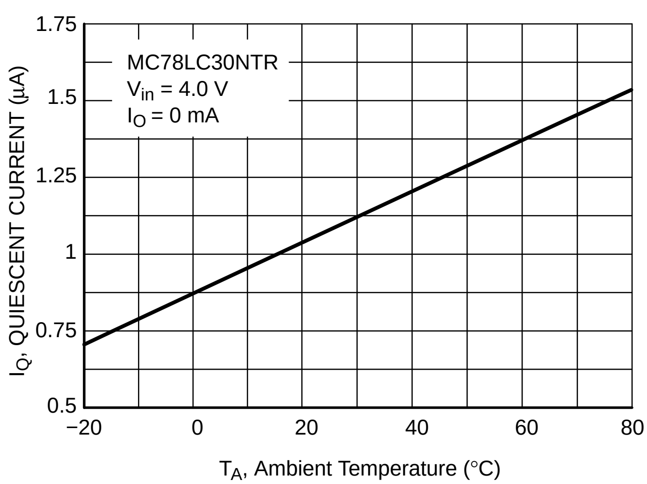


Figure 12. Quiescent Current versus Temperature

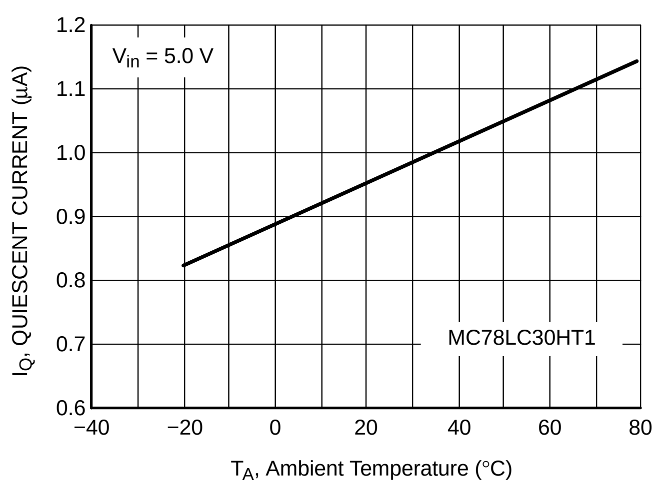


Figure 13. Quiescent Current versus Temperature

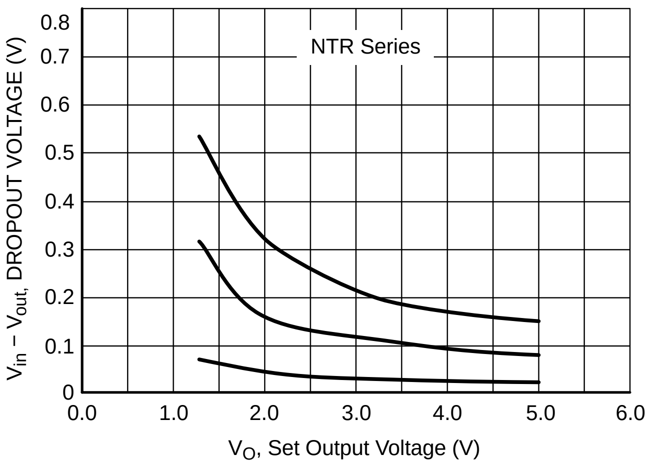


Figure 14. Dropout Voltage versus Set Output Voltage

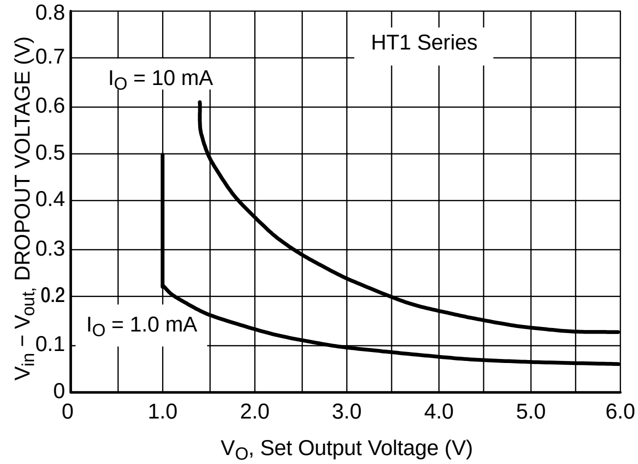


Figure 15. Dropout Voltage versus Set Output Voltage

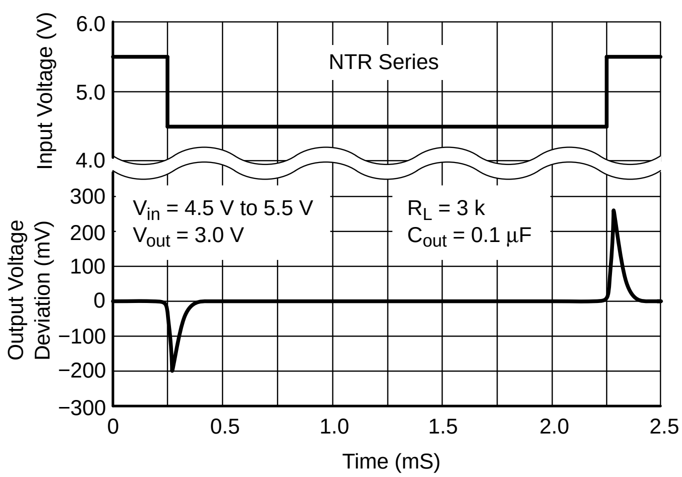


Figure 16. Line Transient

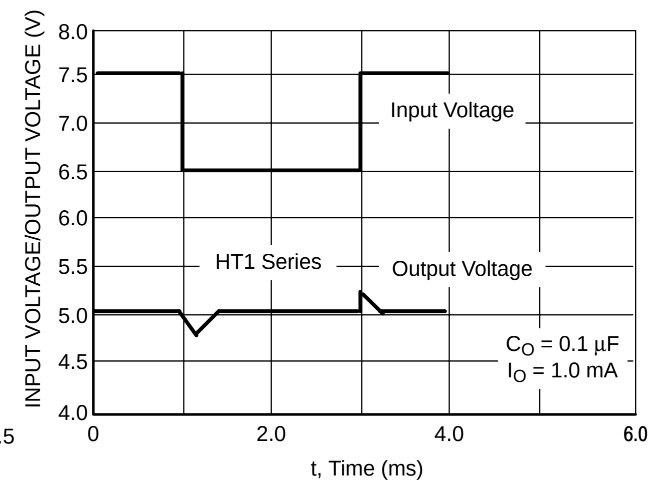


Figure 17. Line Transient Response

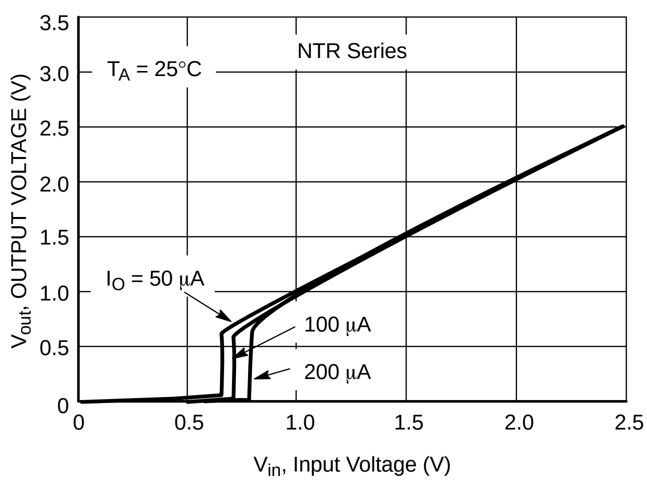


Figure 18. Output Voltage versus Input Voltage

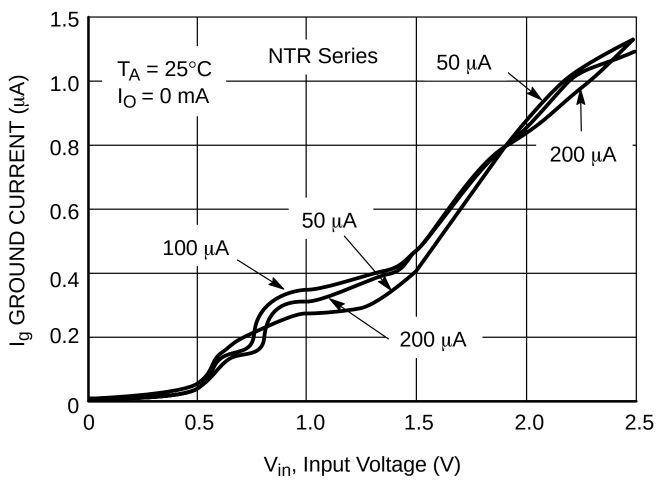


Figure 19. Ground Current versus Input Voltage

APPLICATIONS INFORMATION

A typical application circuit for the MC78LC00 series is shown in Figure 20.

Input Decoupling (C1)

A 0.1 μF capacitor either ceramic or tantalum is recommended and should be connected close to the MC78LC00 package. Higher values and lower ESR will improve the overall line transient response.

Output Decoupling (C2)

The MC78LC00 is a stable component and does not require any specific Equivalent Series Resistance (ESR) or a minimum output current. Capacitors exhibiting ESRs ranging from a few mΩ up to 3.0 Ω can thus safely be used. The minimum decoupling value is 0.1 μF and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load regulation transient response.

Hints

Please be sure the Vin and Gnd lines are sufficiently wide. When the impedance of these lines is high, there is a chance to pick up noise or cause the regulator to malfunction.

Set external components, especially the output capacitor, as close as possible to the circuit, and make leads as short as possible.

Thermal

As power across the MC78LC00 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and also the ambient temperature effect the rate of temperature rise for the part. This is stating that when the MC78LC00 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power dissipation applications.

The maximum dissipation the package can handle is given by:

$$PD = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

If junction temperature is not allowed above the maximum 125°C, then the MC78LC00NTR can dissipate up to 357 mW @ 25°C.

The power dissipated by the MC78LC00NTR can be calculated from the following equation:

$$P_{tot} = [V_{in} * I_{gnd} (I_{out})] + [V_{in} - V_{out}] * I_{out}$$

or

$$V_{inMAX} = \frac{P_{tot} + V_{out} * I_{out}}{I_{gnd} + I_{out}}$$

If an 80 mA output current is needed then the ground current from the data sheet is 1.1 μA. For an MC78LC30NTR (3.0 V), the maximum input voltage will then be 7.4 V.

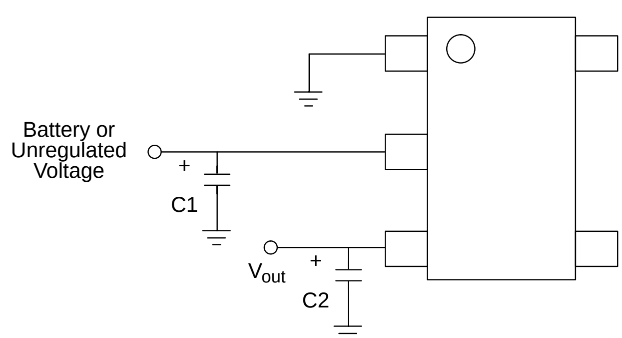


Figure 20. Basic Application Circuit for NTR Suffixes

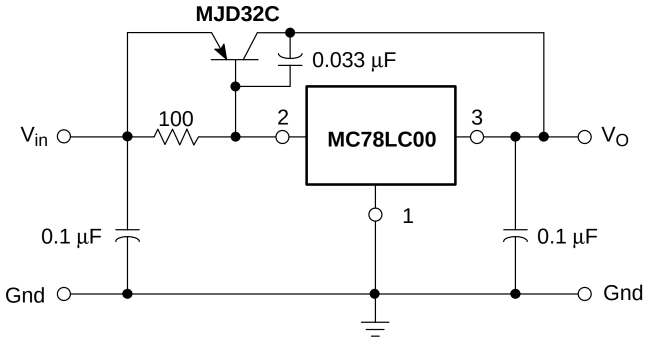


Figure 21. Current Boost Circuit

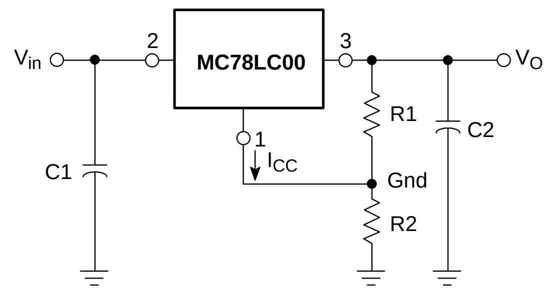


Figure 22. Adjustable V_O

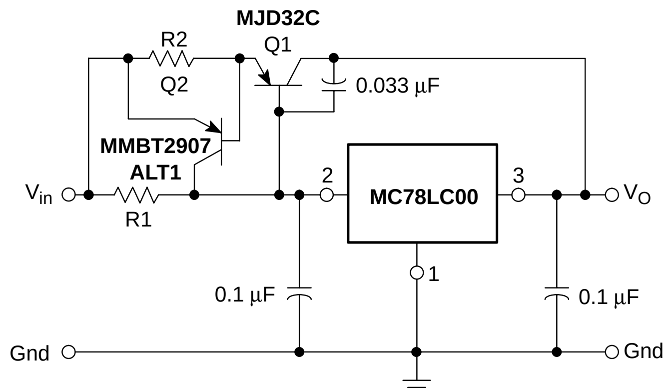


Figure 23. Current Boost Circuit with Overcurrent Limit Circuit

$$V_O = V_{O(Reg)}\left(1 + \frac{R2}{R1}\right) + I_{CC}\,R2$$

$$I_{O(short\ circuit)} \approx \frac{V_{BE2}}{R2} + \frac{V_{BE1} + V_{BE2}}{R1}$$

ORDERING INFORMATION

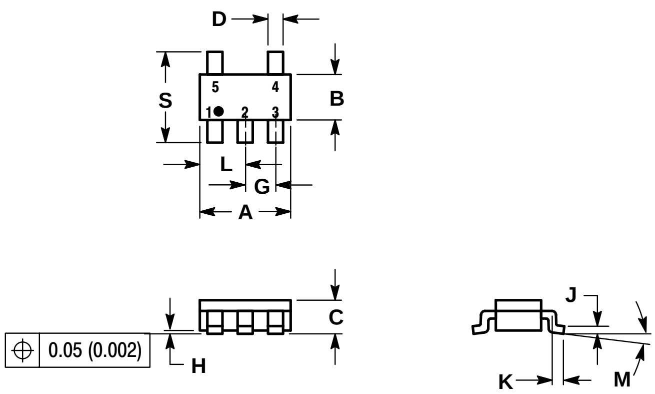
Device	Nominal Output Voltage	Marking	Package	Shipping†
MC78LC15NTR	1.5	LAG	Thin SOT23−5	3000 Units/7″ Tape & Reel
MC78LC15NTRG	1.5	LAG	Thin SOT23−5 (Pb−Free)	
MC78LC18NTR	1.8	LAH	Thin SOT23−5	
MC78LC18NTRG	1.8	LAH	Thin SOT23−5 (Pb−Free)	
MC78LC25NTR	2.5	LAI	Thin SOT23−5	
MC78LC25NTRG	2.5	LAI	Thin SOT23−5 (Pb−Free)	
MC78LC27NTR	2.7	LAJ	Thin SOT23−5	
MC78LC27NTRG	2.7	LAJ	Thin SOT23−5 (Pb−Free)	
MC78LC28NTR	2.8	LAK	Thin SOT23−5	
MC78LC28NTRG	2.8	LAK	Thin SOT23−5 (Pb−Free)	
MC78LC30NTR	3.0	LAL	Thin SOT23−5	
MC78LC30NTRG	3.0	LAL	Thin SOT23−5 (Pb−Free)	
MC78LC33NTR	3.3	LAM	Thin SOT23−5	
MC78LC33NTRG	3.3	LAM	Thin SOT23−5 (Pb−Free)	
MC78LC40NTR	4.0	LEC	Thin SOT23−5	
MC78LC40NTRG	4.0	LEC	Thin SOT23−5 (Pb−Free)	
MC78LC50NTR	5.0	LAN	Thin SOT23−5	
MC78LC50NTRG	5.0	LAN	Thin SOT23−5 (Pb−Free)	
MC78LC30HT1	3.0	0C	SOT−89	1000 Units Tape & Reel
MC78LC30HT1G	3.0	0C	SOT−89 (Pb−Free)	
MC78LC33HT1	3.3	3C	SOT−89	
MC78LC33HT1G	3.3	3C	SOT−89 (Pb−Free)	
MC78LC40HT1	4.0	0D	SOT−89	
MC78LC40HT1G	4.0	0D	SOT−89 (Pb−Free)	
MC78LC50HT1	5.0	0E	SOT−89	
MC78LC50HT1G	5.0	0E	SOT−89 (Pb−Free)	

Additional voltages in 100 mV steps are available upon request by contacting your ON Semiconductor representative.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

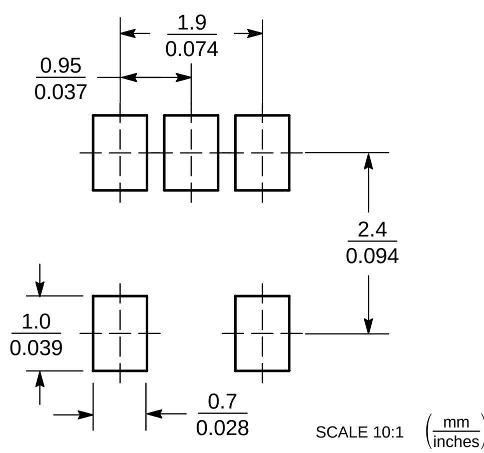
THIN SOT23−5
NTR SUFFIX
PLASTIC PACKAGE
CASE 483−02
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. A AND B DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0 °	10 °	0 °	10 °
S	2.50	3.00	0.0985	0.1181

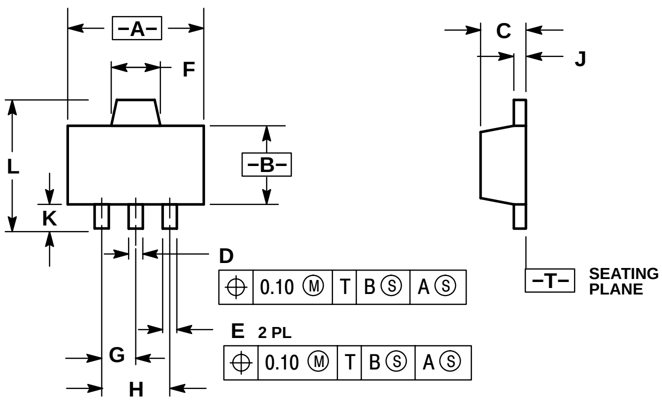
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

SOT−89
H SUFFIX
PLASTIC PACKAGE
CASE 1213−02
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 1213−01 OBSOLETE, NEW STANDARD 1213−02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.40	4.60	0.173	0.181
B	2.40	2.60	0.094	0.102
C	1.40	1.60	0.055	0.063
D	0.37	0.57	0.015	0.022
E	0.32	0.52	0.013	0.020
F	1.50	1.83	0.059	0.072
G	1.50 BSC		0.059 BSC	
H	3.00 BSC		0.118 BSC	
J	0.30	0.50	0.012	0.020
K	0.80	---	0.031	---
L	---	4.25	---	0.167

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