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1 FEATURES

1.1 PCF84CXXXA kernel

- 8-bit CPU, ROM, RAM, I/O in a single 42 leads shrink DIL package
- Over 80 instructions all of 1 or 2 cycles
- 29 quasi bidirectional standard I/O port lines
- Configuration of I/O lines individually selected by mask
- External interrupt $\overline{INT}$/T0
- 2 direct testable inputs T0, T1
- 8-bit programmable timer/event counter
- 3 single level vectored interrupts (external, timer/counter, I^2C-bus)
- Power-on-reset and low voltage detector
- Single power supply
- 2 power reduction modes: Idle and Stop
- Operating temperature range: −20 to +70 °C
- Silicon gate CMOS fabrication process (SAC2).

1.2 Derivative features PCA84C640

Although the **PCA84C640** is specifically referred to throughout this data sheet, the information applies to all the devices. The small differences between the 84C640 and the other devices are specified in the text and also highlighted in Chapter 6.

The PCA84C640 comprises:

- The PCF84CXXXA processor core
- 6 kbytes mask-programmable program ROM
- 128 bytes RAM
- Multi-master I^2C-bus interface
- AFC input for Voltage Synthesized Tuning (VST; with 3-bit DAC and comparator)
- On Screen Display (OSD) facility for two rows of 16-characters
- On Screen Display character set of 64 types
- Four programmable display dot sizes
- Half dot character rounding
- Seven colours for each character
- One 14-bit PWM output for VST
- Five 6-bit PWM outputs for analog controls
- Eight port lines with 10 mA LED drive capability
- 18 general purpose bidirectional I/O lines plus 11 function-combined I/O lines
- 2 direct testable lines
- Programmable VSYNCN and HSYNCN input polarity
- RC oscillator for OSD function.

2 GENERAL DESCRIPTION

The 84C44X; 84C64X; 84C84X denotes the types:

- PCA84C440; 84C441; 84C443; 84C444
- PCA84C640; 84C641; 84C643; 84C644
- PCA84C840; 84C841; 84C843; 84C844,

which are 8-bit microcontrollers with On Screen Display (OSD) and Voltage Synthesized Tuning (VST) functions. All are members of the 84CXXX microcontroller family.

There are two oscillator types for the OSD function in the various types, i.e.,

- RC oscillator: PCA84C440; 84C443; 84C640; 84C643; 84C840; 84C843
- LC oscillator: PCA84C441; 84C444; 84C641; 84C644; 84C841; 84C844.

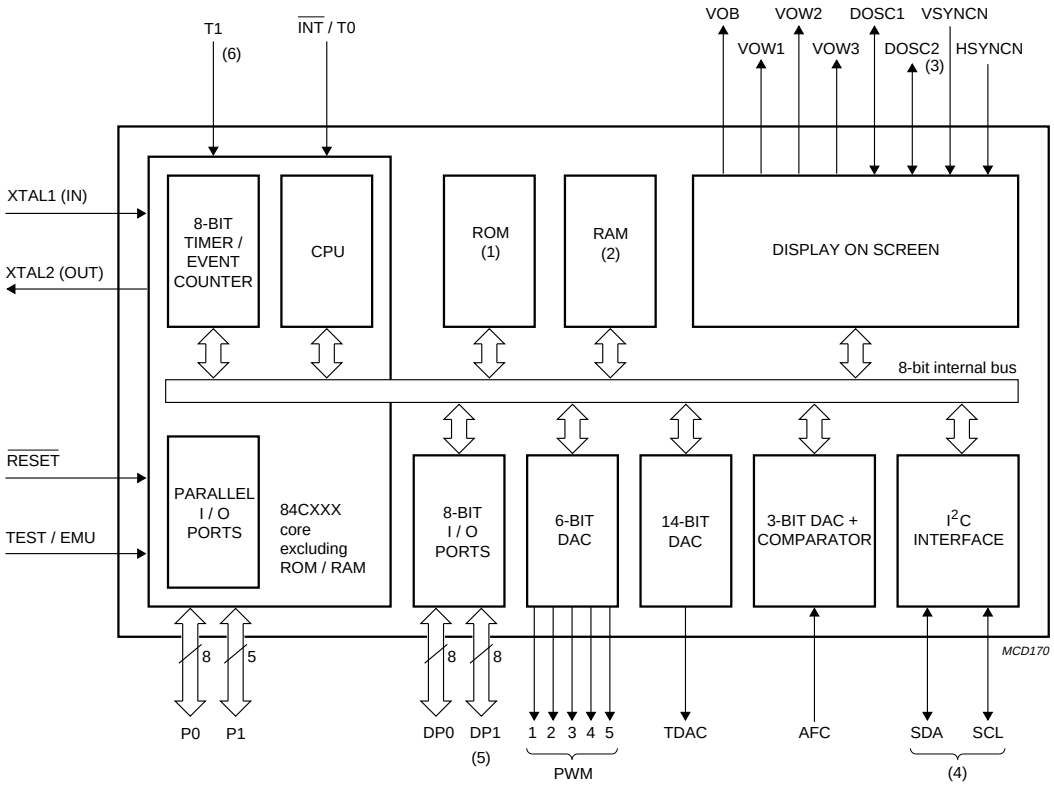
2.1 Important note

This data sheet details the specific properties of the PCA84C44X, PCA84C64X and PCA84C84X.
The shared characteristics of the PCA84CXXX family of microcontrollers are described in the PCF84CXXXA Family single-chip 8-bit Microcontroller of *"Data Handbook IC14"*, which should be read in conjunction with this data sheet.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE			TEMPERATURE RANGE (°C)
	NAME	DESCRIPTION	VERSION	
PCA84C440; 84C443; 84C640; 84C643; 84C840; 84C843	SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1	−20 to +70
PCA84C441; 84C444; 84C641; 84C644; 84C841; 84C844				

4 BLOCK DIAGRAM



(1) 4K bytes for the PCA84C440; 84C441; 84C443; 84C444.
6K bytes for the PCA84C640; 84C641; 84C643; 84C644.
8K bytes for the PCA84C840; 84C841; 84C843; 84C844.

(2) 128 bytes for the PCA84C440; 84C441; 84C443; 84C444; 84C640; 84C641; 84C643; 84C644.
192 bytes for the PCA84C840; 84C841; 84C843; 84C844.

(3) For use with an LC oscillator, only available with the:
PCA84C441; 84C444; 84C641; 84C644; 84C841; 84C844.

(4) I^2C-bus interface not available with the:
PCA84C443; 84C444; 84C643; 84C644; 84C843; 84C844.

(5) DP1.4 only available for PCA84C440; 84C443; 84C640; 84C643; 84C840; 84C843.

(6) T1 = pin 29 for PCA84C440; 84C443; 84C640; 84C643; 84C840; 84C843.
T1 = pin 34 for PCA84C441; 84C444; 84C641; 84C644; 84C841; 84C844.

Fig.1 Block diagram.

5 PINNING INFORMATION

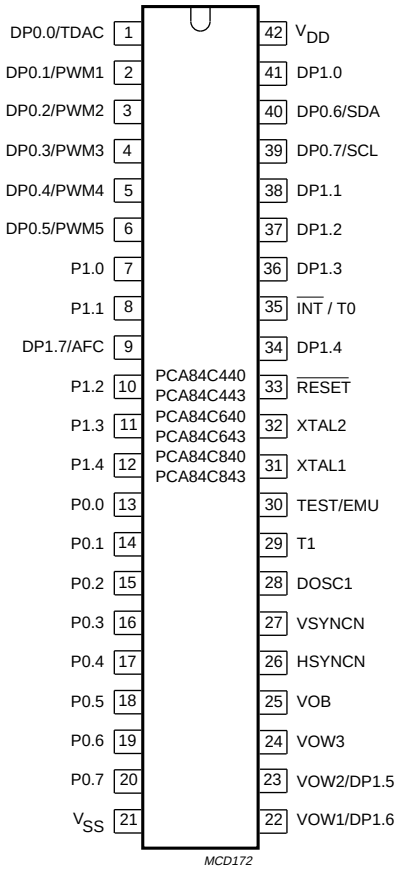


Fig.2 Pinning diagram for PCA84CX40; 84CX43.

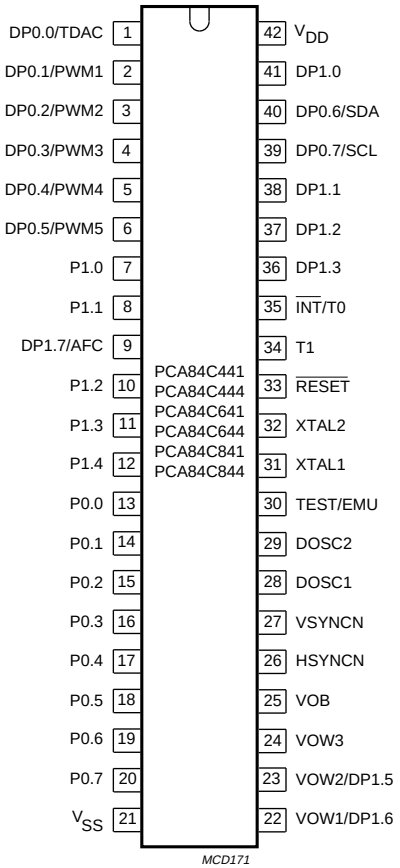


Fig.3 Pinning diagram for PCA84CX41; 84CX44.

Table 1 Pin description

SYMBOL[1]		PIN[1]		DESCRIPTION
84CX40; 84CX43	**84CX41; 84CX44**	**84CX40; 84CX43**	**84CX41; 84CX44**	
Deviating pinning				
DP1.0 to DP1.4	DP1.0 to DP1.3	41, 38, 37, 36, 34	41, 38, 37, 36	Derivative Port 1: quasi-bidirectional I/O lines.
T1	T1	29	34	Direct testable pin and event counter input.
DOSC1	–	28	–	Connection to RC oscillator of OSD clock.
–	DOSC1/DOSC2	–	28, 29	Connections to LC oscillator of OSD clock.
Mutual pinning				
DP0.0/TDAC		1		Derivative Port 0: quasi-bidirectional I/O line or 14-bit DAC PWM.
DP0.1 to DP0.5/PWM1 to PWM5		2 to 6		Derivative Port 1: quasi-bidirectional I/O lines or 6-bit DAC PWM.
P1.0 to P1.4		7, 8, 10, 12		Port 1: quasi-bidirectional I/O lines.
P0.0 to P0.7		13 to 20		Port 0: quasi-bidirectional I/O port.
DP1.7/AFC		9		Derivative Port 1: quasi-bidirectional I/O line or comparator input with 3-bit DAC.
DP0.6/SDA		40		Derivative open drain I/O port or I^2C-bus data line.
DP0.7/SCL		39		Derivative open drain I/O port or I^2C- bus clock line.
$\overline{INT}$/T0		35		External interrupt or direct testable line.
DP1.5 to DP1.6/VOW2 to VOW1		23, 22		Derivative Port 1: quasi-bidirectional I/O lines or character video output.
$\overline{RESET}$		33		Initialize input, active LOW.
XTAL2, XTAL1		32, 31		Oscillator output or input terminal for system clock.
TEST/EMU		30		Control input for testing and emulation mode. Ground for normal operation.
VSYNCN		27		Vertical synchronous signal input.
HSYNCN		26		Horizontal synchronous signal input.
VOB		25		Blanking output.
VOW3		24		Character video output of OSD.
V_{SS}		21		Ground.
V_{DD}		42		Power supply.

Note

1. **84CX40; 84CX43** denotes the types: PCA84C440, PCA84C443, PCA84C640, PCA84C643, PCA84C840 and PCA84C843.
   84CX41; 84CX44 denotes the types: PCA84C441, PCA84C444, PCA84C641, PCA84C644, PCA84C841 and PCA84C844.

6 DIFFERENCES BETWEEN THE TYPES

Table 2 Differences between the types PCA84C44X, PCA84C64X and PCA84C84X

In this table: yes = available; no = not available.

FEATURE	PCA...											
	84C440	**84C441**	**84C443**	**84C444**	**84C640**	**84C641**	**84C643**	**84C644**	**84C840**	**84C841**	**84C843**	**84C844**
OSD oscillator	RC	LC	RC	LC	RC	LC	RC	LC	RC	LC	RC	LC
General purpose I/O lines	18	17	18	17	18	17	18	17	18	17	18	17
I^2C-bus interface	yes	yes	no	no	yes	yes	no	no	yes	yes	no	no
ROM	4 kbytes				6 kbytes				8 kbytes			
RAM	128 bytes				128 bytes				192 bytes			
Pin assignment												
Pin 29	T1	DOSC2	T1	DOSC2	DP1.4	T1	DP1.4	T1	DP1.4	T1	DP1.4	T1
Pin 34	DP1.4	T1	DP1.4	T1	T1	DOSC2	T1	DOSC2	T1	DOSC2	T1	DOSC2
Register DP1 (bit DP1.4)												
Pin	yes	no	yes	no	yes	no	yes	no	yes	no	yes	no
Latch	yes	no	yes	no	yes	no	yes	no	yes	no	yes	no

7 RESET

The $\overline{RESET}$ pin (active LOW input) is used to initialize the microcontroller to a defined state. The Reset configuration is shown in Fig.5.

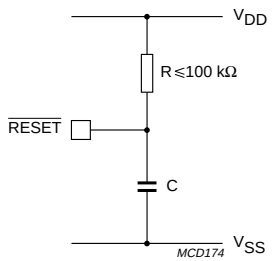


Fig.4 External components for $\overline{RESET}$ pin.

7.1 Power-on-reset

The Power-on-reset circuit monitors the voltage level of V_{DD}. If V_{DD} remains below the internal reference voltage level V_{ref} (typically 1.3 V), the oscillator is inhibited. When V_{DD} rises above V_{ref}, the oscillator is released and the internal reset is active for a period of t_d (typically 50 µs).

Considering the V_{DD} rise time, the following measures for a correct Power-on-reset can be taken:

- If the V_{DD} rises above the minimum operation voltage before time period t_d is exceeded, no external components are necessary (see Fig.6).
- If V_{DD} has a slow rise time, such that after the time period $(t_{Vref} + t_d)$ has elapsed the supply voltage is still below the minimum operation voltage (V_{min}), external components are required (see Figs 4 and 7). To guarantee a correct reset operation, ensure that the time constant $RC \geq 8 \times t_{VDD}$.

A definite Power-on-reset can be realized by applying an (external) $\overline{RESET}$ signal during power-on.

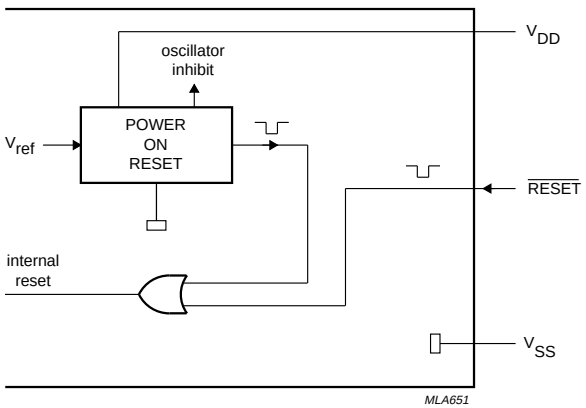


Fig.5 Reset configuration.

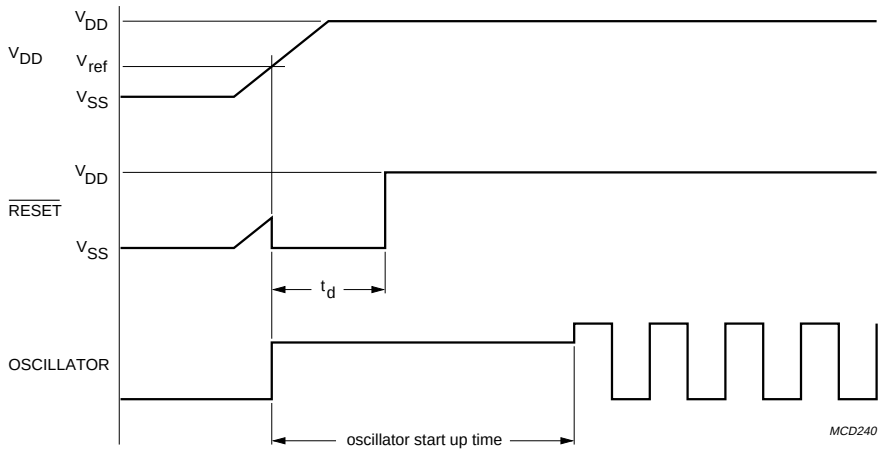


Fig.6 Reset with fast rising V_{DD}.

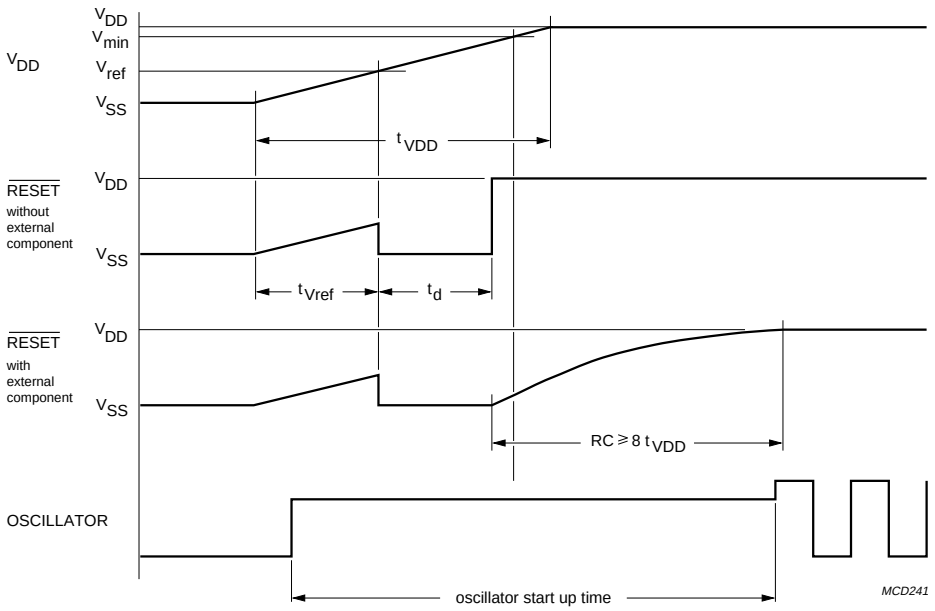


Fig.7 Reset with slow V_{DD}.

8 ANALOG CONTROL

8.1 6-bit PWM DACs

Five PWM outputs are available for analog control purposes e.g. volume, balance, brightness, saturation etc. The block diagram of a typical 6-bit PWM DAC is shown in Fig.8. Each PWM output can generate pulses of programmable length that have a repetition frequency of $\frac{1}{64} \times f_{PWM}$, where $f_{PWM} = \frac{1}{3} \times f_{XTAL}$.

8.1.1 PIN SELECTION FOR PWM OUTPUTS

The PWM outputs **PWM1 to PWM5**, share the same pins as the **Derivative Port lines DP0.1 to DP0.5**.

Setting the (relevant PWM enable) bit PWMnE to:

- Logic 1, selects the relevant PWMx output function
- Logic 0, selects the relevant DP0.x Port function.

8.1.2 POLARITY OF THE PWM OUTPUTS

The polarity of all five PWM outputs is selected by the state of the polarity control bit P6LVL.

Setting the control bit P6LVL to:

- Logic 0, sets the PWMx outputs to the default polarity
- Logic 1, inverts all the PWMx outputs.

8.1.3 ANALOG OUTPUT VOLTAGE

A DC voltage proportional to the PWM control setting may be obtained by connecting an integrating network to each of the PWM outputs (see Fig.9).

The analog value is calculated as follows:

$$V_A = \frac{t_{HIGH}}{t_r} \times V_O$$

Where:

- $t_{HIGH} = t_0 \times PWMDL$ = HIGH time of the PWM pulse
- $t_r = t_0 \times 64$ = repetition time of the PWM pulse
- $t_0 = \frac{3}{f_{XTAL}}$
- PWMDL is the decimal value of the contents of the PWM data latch.

Therefore, the analog output voltage is:

$$V_A = \frac{PWMDL}{64} \times V_O$$

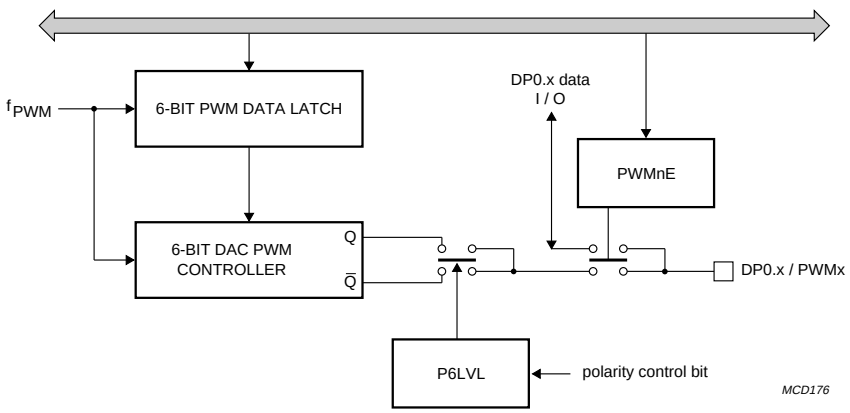


Fig.8 Block diagram of the 6-bit PWM DAC.

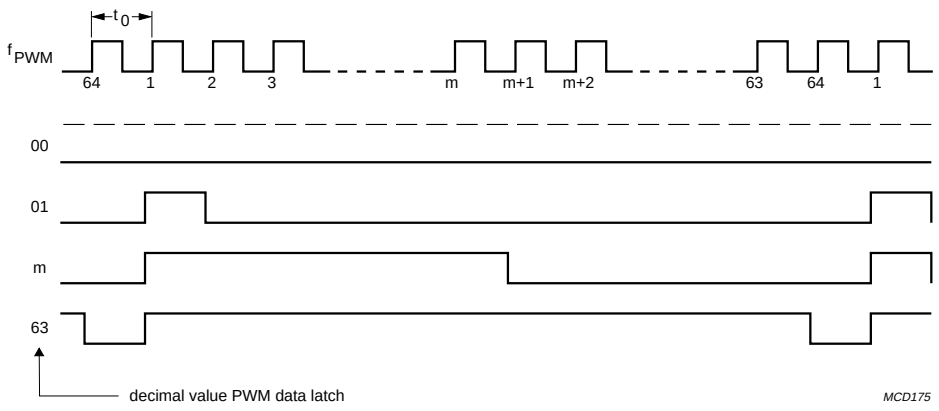


Fig.9 PWM output patterns (P6LVL = 0).

9 VST CONTROL

9.1 14-bit PWM DAC

The PCA84C640 has one 14-bit PWM DAC output (TDAC) with a resolution of 16384 levels for Voltage Synthesized Tuning. The PWM DAC (see Fig.10) consists of:

- 14-bit counter
- Two 7-bit DAC interface data latches (VSTH and VSTL)
- One 14-bit DAC data latch (VSTREG)
- Pulse control.

The polarity of output TDAC is selected with bit P14LVL. Setting the bit P14LVL to:

- Logic 1, sets the TDAC output to the default polarity
- Logic 0, inverts the TDAC output.

9.1.1 14-BIT COUNTER

The counter is continuously running and is clocked by f_0.

The period of the clock, $t_0 = \frac{3}{f_{XTAL}}$

The repetition time for one complete cycle of the counter:

$$t_r = t_0 \times 16384$$

The repetition time for one cycle of the lower 7-bits of the counter is:

$$t_{sub} = t_0 \times 128$$

Therefore, the number of t_{sub} periods in a complete cycle t_r is:

$$N = \frac{t_0 \times 16384}{t_0 \times 128} = 128$$

9.1.2 DATA AND INTERFACE LATCHES

In order to ensure correct operation, interface data latch VSTH is loaded first and then interface data latch VSTL. The contents of:

- VSTH are used for coarse adjustment
- VSTL are used for fine adjustment.

At the beginning of the first t_{sub} period following the loading of VSTL, both data latches are loaded into data latch VSTREG. After the contents of VSTH and VSTL are latched into VSTREG, one t_{sub} period is needed to generate the appropriate pulse pattern.
To ensure correct DAC conversion, two (2) t_{sub} periods should be allowed before beginning the next sequence.

9.2 Coarse adjustment

The coarse adjustment output (OUT1) is reset to LOW (inactive) at the start of each t_{sub} period.
It will remain LOW until the time $[t_0 \times (VSTH + 1)]$ has elapsed and then will go HIGH and remain so until the next t_{sub} period starts.

9.3 Fine adjustment

Fine adjustment is achieved by generating additional pulses at the start of particular sub-periods (t_{subn}).
These additional pulses have a width of t_0.
The sub-period in which a pulse is added is determined by the contents of VSTL interface latch.
Table 3 gives the numbers of the t_{subn}, at the start of which an additional pulse is generated, depending on the bit in VSTL being a logic 0. When more than one bit is a logic 0 a combination of additional pulses are generated.
For example, if VSTL = 1111010, which is a combination of

- VSTL = 1111110: sub-period 64, and
- VSTL = 1111011: sub-periods 16, 48, 80, 112,

then additional pulses will be given in sub-periods 16, 48, 64, 80 and 112; this is illustrated in Fig.12.

If VSTH = 0011101, VSTL = 1111010 and P14LVL = 0, then the TDAC output is as shown in Fig.13.

Table 3 Additional pulse distribution

LOWER 7 BITS (VSTL)	ADDITIONAL PULSE IN SUB-PERIODS t_{subn}
111 1110	64
111 1101	32, 96
111 1011	16, 48, 80, 112
111 0111	8, 24, 40, 56, 72, 88, 104, 120
110 1111	4, 12, 20, 28, 36, 44, 52, 60 .... 116, 124
101 1111	2, 6, 10, 14, 18, 22, 26, 30, ... 122, 126
011 1111	1, 3, 5, 7, 9, 11, 13, 15, 17, ... 125, 127

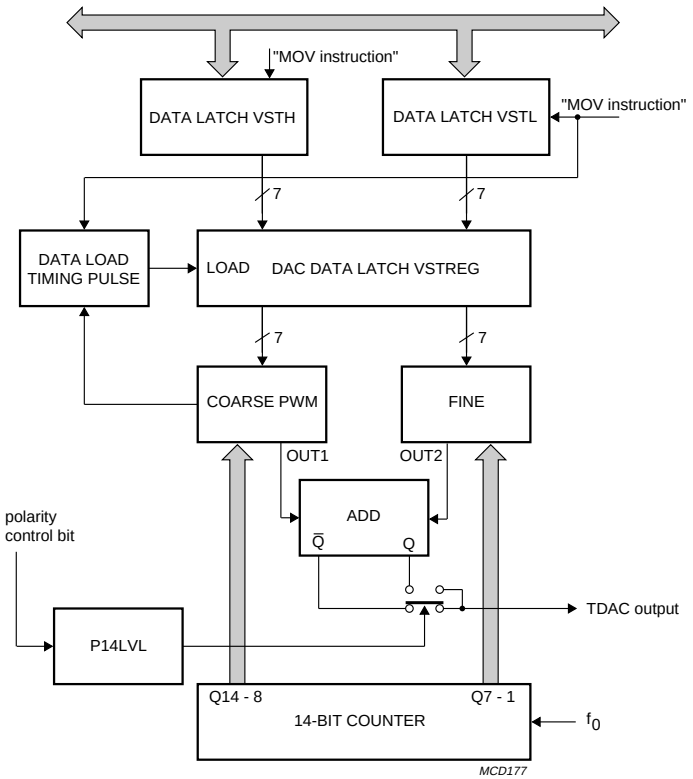


Fig.10 Block diagram of the 14-bit PWM DAC.

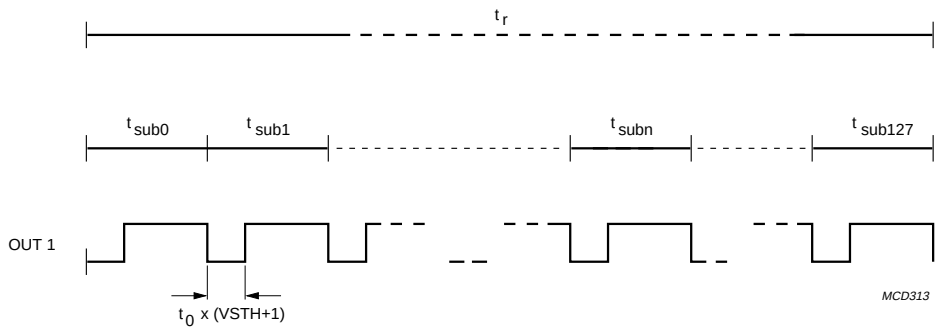


Fig.11 Coarse adjustment output (OUT1).

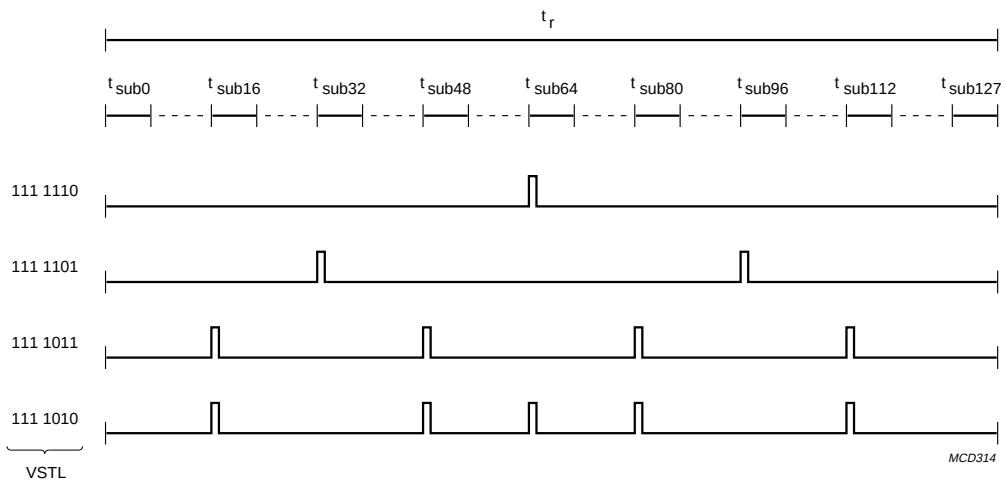


Fig.12 Fine adjustment output (OUT2).

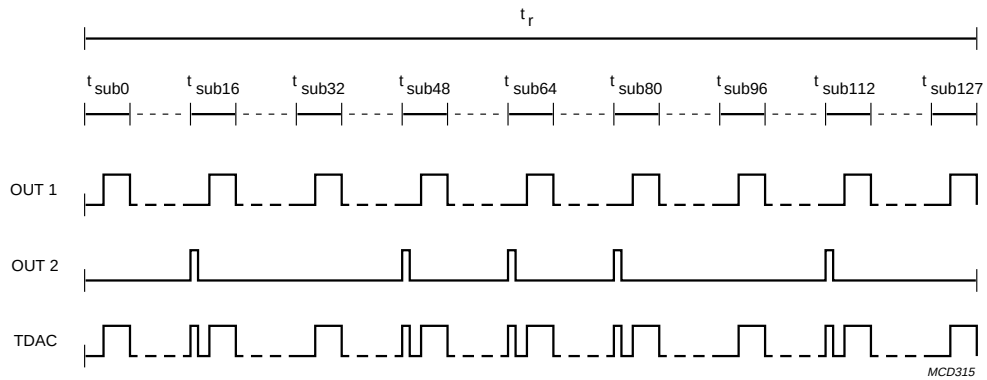


Fig.13 TDAC output.

10 AFC INPUT

The AFC input is used to measure the level of the Automatic Frequency Control signal. This is achieved by comparing the AFC input signal with the output of a 3-bit DAC as shown in Fig.14. DAC analog switches select one of 8 resistor taps connected between V_{DD} and V_{SS}. Consequently, eight different voltages may be selected (see Table 4). The compare signal AFCC, can be tested to determine whether the AFC input is higher or lower than the DAC level.

The AFC input shares the same pin as the Derivative Port line DP1.7. Setting the enable bit AFCE to:

- Logic 1, selects the AFC function
- Logic 0, selects the Derivative Port DP1.7 function.

Table 4 Selection of V_{ref}

AFC2	AFC1	AFC0	V_{ref}	V_{ref} (for V_{DD} = 5.0 V)
0	0	0	$V_{DD} \times 0.125$	0.625 V
0	0	1	$V_{DD} \times 0.250$	1.250 V
0	1	0	$V_{DD} \times 0.375$	1.875 V
0	1	1	$V_{DD} \times 0.500$	2.500 V
1	0	0	$V_{DD} \times 0.625$	3.125 V
1	0	1	$V_{DD} \times 0.750$	3.750 V
1	1	0	$V_{DD} \times 0.875$	4.375 V
1	1	1	V_{DD}	5.000 V

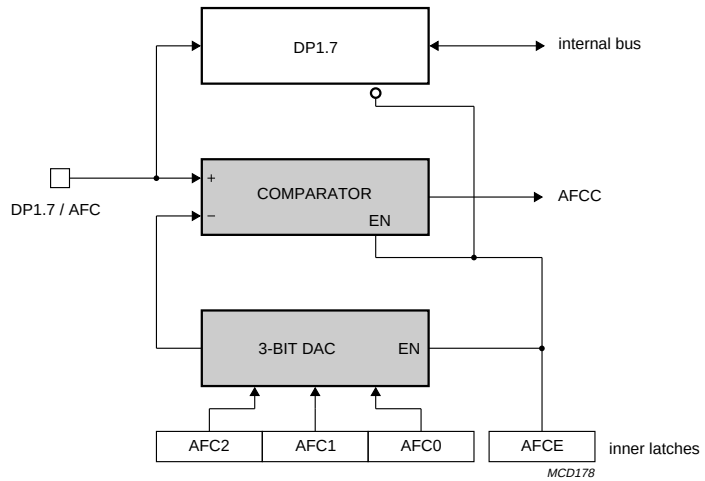


Fig.14 AFC circuit.

11 INPUT/OUTPUT (I/O)

Each parallel I/O port line may be individually configured using one of three possible I/O mask options.
The three I/O mask options are specified below:

Option 1 Standard port with switched pull-up current source, Fig.15.

Option 2 Open drain, Fig.16.

Option 3 Push-pull (output only), Fig.17.

Table 5 specifies the possible port option list. When these devices are used for emulation purposes, in order to match the piggy back device provided it is recommended that the port options listed in Table 6 are used.

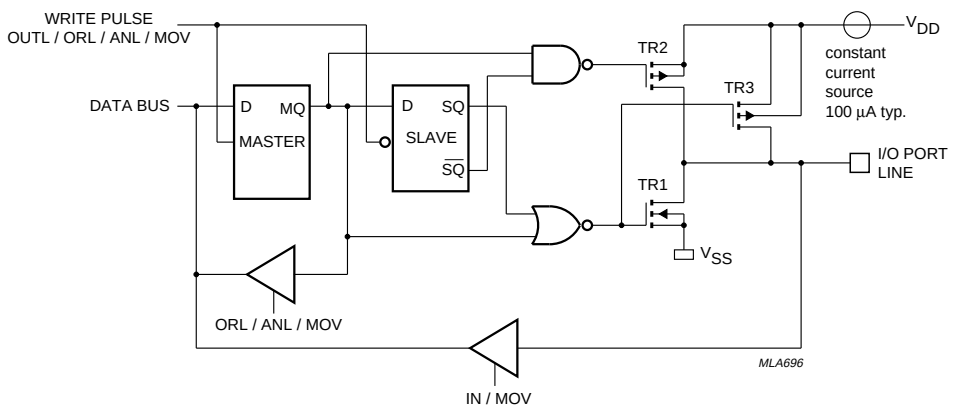


Fig.15 Standard output with switched pull-up current source (Option 1).

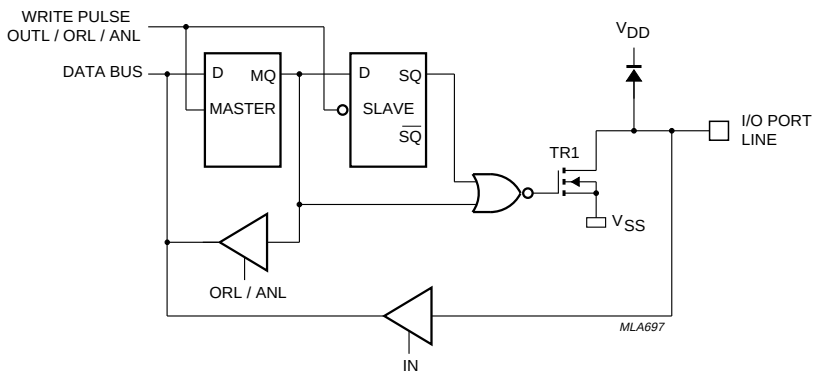


Fig.16 Open drain type I/O (Option 2).

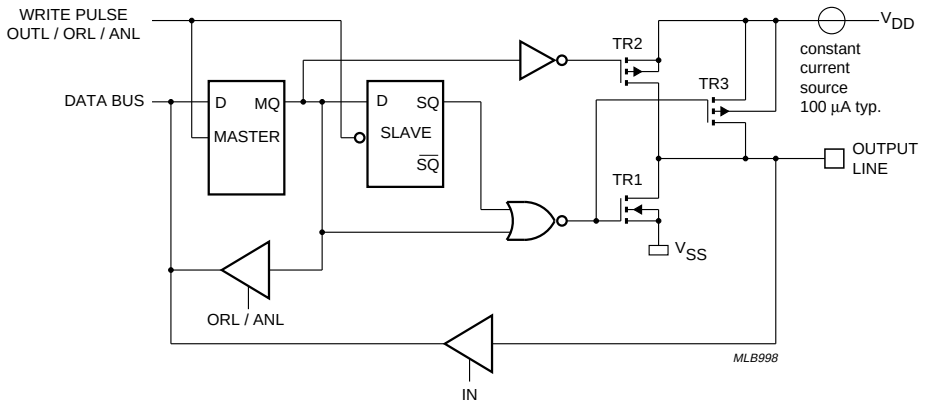


Fig.17 Push-pull type output (Option 3).

Table 5 User mask programmable port option list

PORT	PIN	OPTION[1]	
P0.0	13		
P0.1	14		
P0.2	15		
P0.3	16		
P0.4	17		
P0.5	18		
P0.6	19		
P0.7	20		
P1.0	7		
P1.1	8		
P1.2	10		
P1.3	11		
P1.4	12		
DP0.0	1		
DP0.1	2		
DP0.2	3		
DP0.3	4		
DP0.4	5		
DP0.5	6		
DP0.6	40		
DP0.7	39		
DP1.0	41		
DP1.1	38		
DP1.2	37		
DP1.3	36		
DP1.4[2]	34		
DP1.5	23		
DP1.6	22		
DP1.7	9		
VOB	25	3	R
VOW3	24	3	R

Table 6 Port options for the 84C640 in emulation mode

PORT	PIN	OPTION	
P0.0	13	1	S
P0.1	14	1	S
P0.2	15	1	S
P0.3	16	1	S
P0.4	17	1	S
P0.5	18	1	S
P0.6	19	1	S
P0.7	20	1	S
P1.0	7	1	S
P1.1	8	1	S
P1.2	10	1	S
P1.3	11	1	S
P1.4	12	1	S
DP0.0	1		
DP0.1	2		
DP0.2	3		
DP0.3	4		
DP0.4	5		
DP0.5	6		
DP0.6	40	2	S
DP0.7	39	2	S
DP1.0	41		
DP1.1	38		
DP1.2	37		
DP1.3	36		
DP1.4	34		
DP1.5	23		
DP1.6	22		
DP1.7	9		
VOB	25	3	R
VOW3	24	3	R

Notes

1. Each pin can be configured to a HIGH (S) or LOW (R) state after power-on-reset. The required state of each pin is therefore specified by R or S.
2. DP1.4 available only with the PCA84C440, PCA84C443, PCA84C640, PCA84C643, PCA84C840 and PCA84C843.

12 ON SCREEN DISPLAY

12.1 Features

- Display format: 2 rows × 16 characters
- Software controlled vertical and horizontal display position
- 64 different (mask programmable) characters in ROM
- Black box background
- Four programmable display character sizes
- Four programmable character dot matrix sizes:
  - 6 × 9 and 6 × 13
  - 8 × 9 and 8 × 13
- Half-dot rounding for the whole screen
- 4 from 7 colours possible on screen
- Clock generator for on screen display function with:
  - RC oscillator
  - LC oscillator,

  for the various types of PCA84C44X; 84C64X; 84C84X.

12.2 Horizontal display position control

The horizontal position counter is incremented every OSD cycle after the programmed level of HSYNCN occurs at the HSYNCN pin. The counter is reset when the opposite polarity of the HSYNCN pulse is reached.

12.3 Vertical display position control

The vertical position counter is incremented every HSYNCN cycle and is reset by the VSYNCN signal.

12.4 Clock generator

There are two types of oscillators available for the various types. The oscillator is triggered on the trailing edge of HSYNCN when the OSD logic is enabled and stops on the following leading edge of HSYNCN.

The OSD oscillator must be externally adjusted to the desired frequency (decreasing the OSD frequency gives broader characters). Before the oscillation frequency can be adjusted HSYNCN must be HIGH (if HLVL = 1). Oscillation stops by setting the HSYNCN pin LOW when HLVL = 1.

12.4.1 RC OSCILLATOR

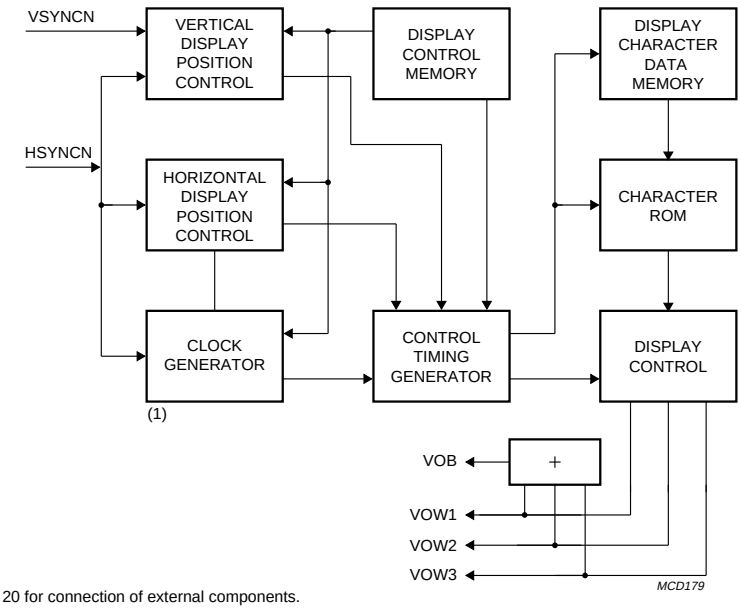
The RC oscillator is available in the types: PCA84C440; 84C443; 84C640; 84C643; 84C840; 84C843.

The external RC network is connected between pin 28 and V_{SS} (see Fig.19).

12.4.2 LC OSCILLATOR

The LC oscillator is available in the types: PCA84C441; 84C444; 84C641; 84C644; 84C841; 84C844.

The external LC network is connected between pins 28 and 29 (see Fig.20).



(1) See Figs 19 and 20 for connection of external components.

Fig.18 OSD block diagram.

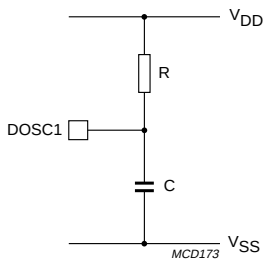


Fig.19 RC oscillator.

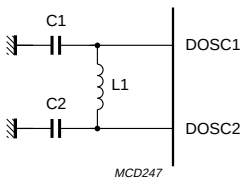


Fig.20 LC oscillator.

12.5 Display data registers

The display data registers consists of a group of 32 derivative registers located at addresses 20H to 3FH inclusive (see Table 7). At power-up the contents of the display data registers are undefined.
The format of each display data register is shown in Table 8, and their functions described in Table 9.

Table 7 Display data registers addresses

ADDRESS	DISPLAY DATA FOR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
20H to 2FH	Row 0 = the first display row	CC1	CC0	MD5	MD4	MD3	MD2	MD1	MD0
30H to 3FH	Row 1 = the second display row								

Table 8 Display data register (address 20H to 3FH)

7	6	5	4	3	2	1	0
CC1	CC0	MD5	MD4	MD3	MD2	MD1	MD0

Table 9 Description of display data register bits

BIT	SYMBOL	FUNCTION
7	CC1	**Colour code**. The state of these two bits enable individual characters to be displayed in one of four colours. See Tables 24, 25 and 26.
6	CC0	
5	MD5	**Character code**. The character set is stored in ROM and consists of 64 different characters. The selection of each character is dependent on the state of the 6 bits, MD0 to MD5.
4	MD4	
3	MD3	
2	MD2	
1	MD1	
0	MD0	

12.6 Display control registers

The display control registers consists of a group of 6 derivative registers located at addresses 40H to 45H inclusive (see Table 10). Each register may be read from or written to. After a reset operation the contents of the display control registers are zero.

Table 10 Display control registers addresses

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
40H	OSDCA	CC34	CC24	CC14	RBLK	ROUND	STBY	VLVL	HLVL
41H	LINE 0A	SZ01	SZ00	VP05	VP04	VP03	VP02	VP01	VP00
42H	LINE 0B	BLK0	VB0	HP05	HP04	HP03	HP02	HP01	HP00
43H	OSDCB	CDTW	CDTH	CC33	CC23	CC32	CC12	CC21	CC11
44H	LINE 1A	SZ11	SZ10	VP15	VP14	VP13	VP12	VP11	VP10
45H	LINE 1B	BLK1	VB1	HP15	HP14	HP13	HP12	HP11	HP10

12.6.1 DERIVATIVE REGISTER OSDCA

Table 11 Derivative register OSDCA (address 40H)

7	6	5	4	3	2	1	0
CC34	CC24	CC14	RBLK	ROUND	STBY	VLVL	HLVL

Table 12 Description of OSCDA bits

BIT	SYMBOL	FUNCTION
7	CC34	**Character colour code bits.** These bits are used for colour selection purposes. See Table 24.
6	CC24	
5	CC14	
4	RBLK	**Raster blanking control** (see Fig.24). When the RBLK bit is: Logic 1, the VOB output is driven HIGH to display the OSD characters on a blank screen. Logic 0, the VOB output returns to its normal output state on the trailing edge of VSYNCN.
3	ROUND	**Character rounding control** (see Figs 22 and 23). The rounding function generates half dots where the corners of two dots meet. The rounding function also works with multiple cell characters. When the ROUND bit is: Logic 1, the rounding function is enabled. Logic 0, the rounding function is disabled.
2	STBY	**Stand-by.** This bit is used to enable or disable the OSD facility. When the STBY bit is: Logic 1, the OSD oscillator is disabled. Logic 0, the OSD oscillator is enabled and the OSD facility is available.
1	VLVL	**Vertical synchronous signal level** (see Fig.21). This bit selects the active level of the VSYNCN input signal. When the VLVL bit is: Logic 1, VSYNCN is active HIGH. Logic 0, VSYNCN is active LOW.
0	HLVL	**Horizontal synchronous signal level** (see Fig.21). This bit selects the active level of the HSYNCN input signal. When the HLVL bit is: Logic 1, HSYNCN is active HIGH. Logic 0, HSYNCN is active LOW.

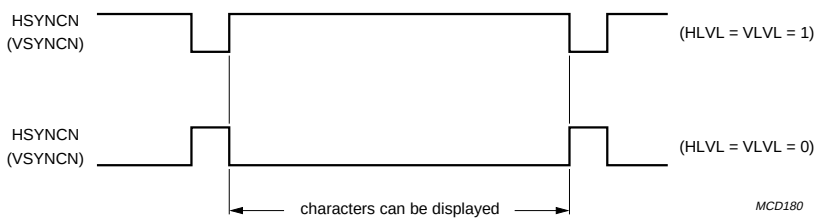


Fig.21 VSYNCN and HSYNCN active level.

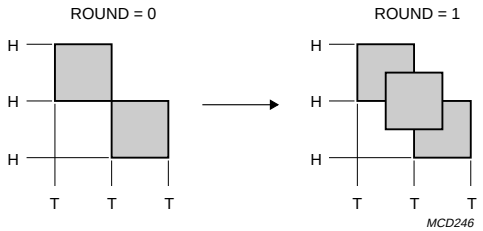


Fig.22 Rounding function.

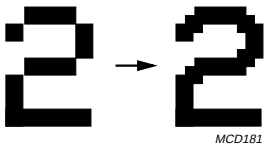


Fig.23 Rounding effect.

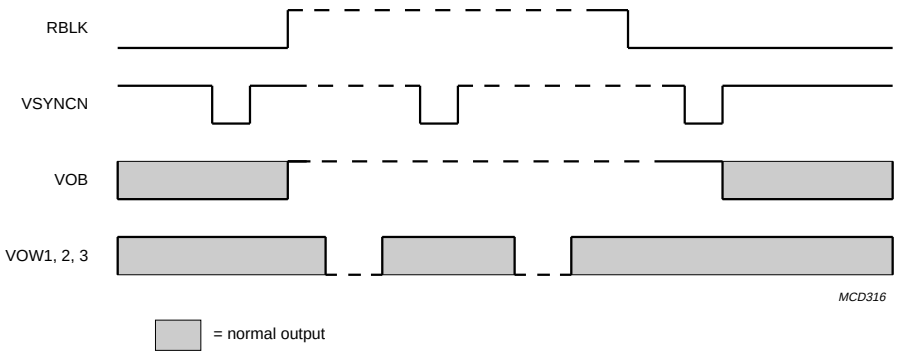


Fig.24 Raster blanking timing RLBK.

12.6.2 DERIVATIVE REGISTERS LINE 0A AND LINE 0B

REGISTER	FUNCTION
LINE 0A	Determine the character size and vertical position of Row 0 (the first display row).
LINE 0B	Determine the horizontal position of Row 0 and the selection of background and blanking functions.

Table 13 Derivative register LINE 0A (address 41H)

7	6	5	4	3	2	1	0
SZ01	SZ00	VP05	VP04	VP03	VP02	VP01	VP00

Table 14 Description of LINE 0A bits

BIT	SYMBOL	FUNCTION
7	SZ01	**Character size.** The state of these two bits enable one of four possible character sizes to be selected for Row 0. Character sizes include background. See Table 23.
6	SZ00	
5	VP05	**Vertical position control.** The vertical position of Row 0 is selected by the state of the 6 bits, VP00 to VP05. For details see Section 12.7.1 “Vertical position”.
4	VP04	
3	VP03	
2	VP02	
1	VP01	
0	VP00	

Table 15 Derivative register LINE 0B (address 42H)

7	6	5	4	3	2	1	0
BLK0	VB0	HP05	HP04	HP03	HP02	HP01	HP00

Table 16 Description of LINE 0B bits

BIT	SYMBOL	FUNCTION
7	BLK0	**Blanking**. This bit enables or disables the character display. When BLK0 is set to: Logic 1, the outputs VOW1, VOW2, VOW3 and VOB are enabled; characters are displayed. Logic 0, the outputs VOW1, VOW2, VOW3 and VOB are disabled; no characters are displayed.
6	VB0	**Background.** This bit determines whether the background display is selected or not. The visual effect of background versus no background is shown in Fig.26. When VB0 is set to: Logic 1, the characters in this row are displayed with background. Logic 0, the background is disabled and only the characters are displayed.
5	HP05	**Horizontal position control**. These 6 bits determine the start position of Row 0. The horizontal position control is only active during OSDC clock cycles. For details Section 12.7.2 “Horizontal position” and Fig.25.
4	HP04	
3	HP03	
2	HP02	
1	HP01	
0	HP00	

12.6.3 DERIVATIVE REGISTERS LINE 1A AND LINE 1B

REGISTER	FUNCTION
LINE 1A	Determine the character size and vertical position of Row 1 (the second display row).
LINE 1B	Determine the horizontal position of Row 1 and the selection of background and blanking functions.

Table 17 Derivative register LINE 1A (address 44H)

7	6	5	4	3	2	1	0
SZ11	SZ10	VP15	VP14	VP13	VP12	VP11	VP10

Table 18 Description of LINE 1A bits

BIT	SYMBOL	FUNCTION
7	SZ11	**Character size.** The state of these two bits enable one of four possible character sizes to be selected for Row 1. Character sizes include background. See Table 23.
6	SZ10	
5	VP15	**Vertical position control.** The vertical position of Row 1 is selected by the state of the 6 bits, VP10 to VP15. For details see Section 12.7.1 “Vertical position”.
4	VP14	
3	VP13	
2	VP12	
1	VP11	
0	VP10	

Table 19 Derivative register LINE 1B (address 45H)

7	6	5	4	3	2	1	0
BLK1	VB1	HP15	HP14	HP13	HP12	HP11	HP10

Table 20 Description of LINE 1B bits

BIT	SYMBOL	FUNCTION
7	BLK1	**Blanking.** This bit enables or disables the character display. When BLK1 is: Logic 0, the outputs VOW1, VOW2, VOW3 and VOB are disabled; no characters are displayed. Logic 1, the outputs VOW1, VOW2, VOW3 and VOB are enabled; characters are displayed.
6	VB1	**Background**. This bit determines whether the background display is selected or not. The visual effect of background versus no background is shown in Fig.26. When VB1 is set to: Logic 1, the characters in this line are displayed with background. Logic 0, the background is disabled and only the character is displayed.
5	HP15	**Horizontal position control**. These 6 bits determine the start position of Row 1. The horizontal position control is only active during OSDC clock cycles. For details Section 12.7.2 “Horizontal position” and Fig.25.
4	HP14	
3	HP13	
2	HP12	
1	HP11	
0	HP10	

12.6.4 DERIVATIVE REGISTER OSDCB

REGISTER	FUNCTION
OSDCB	Determine the selection of: • The size of the dot matrix grid • Four colours from a possible seven for the display.

Table 21 Derivative register OSDCB (address 43H)

7	6	5	4	3	2	1	0
CDTW	CDTH	CC33	CC23	CC32	CC12	CC21	CC11

Table 22 Description of OSDCB bits

BIT	SYMBOL	FUNCTION
7	CDTW	**Character dot width control**.The state of this bit determines the dot width of the character. When the CDTW bit is set to: Logic 1, the character width is 6 dots. Logic 0, the character width is 8 dots.
6	CDTH	**Character dot height control**. The state of this bit determines the dot height of the character. When the CDTH bit is set to: Logic 1, the character height is 13 dots. Logic 0, the character height is 9 dots.
5	CC33	**Colour control bits.** In every VSYNCN cycle one screen can select any 4 colours from 7 and in addition a blank or black screen. Combinations of CC1X, CC2X and CC3X control the character outputs VOW1, VOW2 and VOW3 as shown in Table 24.
4	CC23	
3	CC32	
2	CC12	
1	CC21	
0	CC11	

12.7 OSD display position

12.7.1 VERTICAL POSITION

The line number of the vertical start position for:

- Row 0 is $4 \times (VP00 \rightarrow VP05)$
- Row 1 is $4 \times (VP10 \rightarrow VP15)$.

Where:

- $(VP00 \rightarrow VP05)$ = the decimal value of $VP00 \rightarrow VP05$
- $(VP10 \rightarrow VP15)$ = the decimal value of $VP10 \rightarrow VP15$.

The character height in:

- Row 0 is H0 and is a function of the number of dots per character and the state of the size control bits SZ00 and SZ01
- Row 1 is H1 and is a function of the number of dots per character and the state of the size control bits SZ10 and SZ11.

Row 0 and Row 1 must not overlap each other and therefore: $VP1 \geq (VP0 + H0)$; see Fig.25.

The four possible character heights are shown in Table 23.

12.7.2 HORIZONTAL POSITION

The horizontal start position (HP) of,

- Row 0: $HP0 = 4 \times (HP00 \rightarrow HP05) + 5 \times t_{OSCD}$
- Row 1: $HP1 = 4 \times (HP10 \rightarrow HP15) + 5 \times t_{OSCD}$

Where:

- $(HP00 \rightarrow HP05)$ = the decimal value of $HP00 \rightarrow HP05$ and $(HP00 \rightarrow HP05) > 10$
- $(HP10 \rightarrow HP15)$ = the decimal value of $HP10 \rightarrow HP15$ and $(HP10 \rightarrow HP15) > 10$
- t_{OSCD} = one OSCD clock period.

Therefore for both Row 0 and Row 1,

$HP0, HP1 \geq 45 \times t_{OSCD}$.

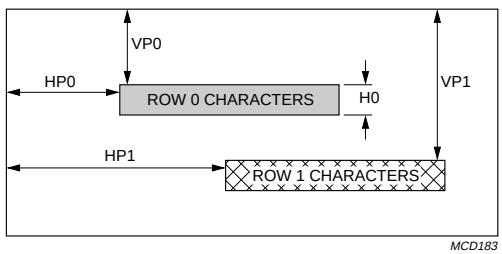


Fig.25 Display position.

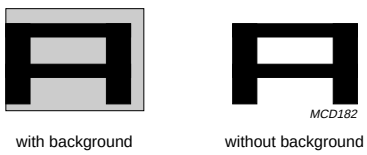


Fig.26 Background versus no background.

12.8 OSD character size and colour selection

12.8.1 CHARACTER SIZE

The character sizes are determined by the bits:

- CDTW, for the width
- CDTH, for the height.

The character sizes are selected by bits SZn1 and SZn0, which denotes:

- SZ01 and SZ00 for Row 0
- SZ11 and SZ10 for Row 1.

Table 23 Character sizes selection

H denotes one horizontal line, T denotes one OSDC clock period and D denotes dots per character width/height.

SIZE BITS		CHARACTER SIZE				DOT MATRIX POINT	
SZn1	SZn0	VERTICAL		HORIZONTAL		VERTICAL	HORIZONTAL
		9D	13D	6D	8D		
0	0	18H	26H	12T	16T	2H	2T
0	1	36H	52H	24T	32T	4H	4T
1	0	54H	78H	36T	48T	6H	6T
1	1	72H	104H	48T	64T	8H	8T

12.8.2 COLOUR SELECTION

Colour selection is achieved using bits in the,

- OSDCA register: CC34, CC24 and CC14
- OSDCB register: CC33, CC23, CC32, CC12, CC21, and CC11
- Display data registers: CC1 and CC0.

In this way every combination of four colours can be made (black and white can not be displayed at the same time). The user may choose one colour out of each block. Table 24 shows the selection of the output combinations. Tables 25 and 26 show the possible colour combinations.

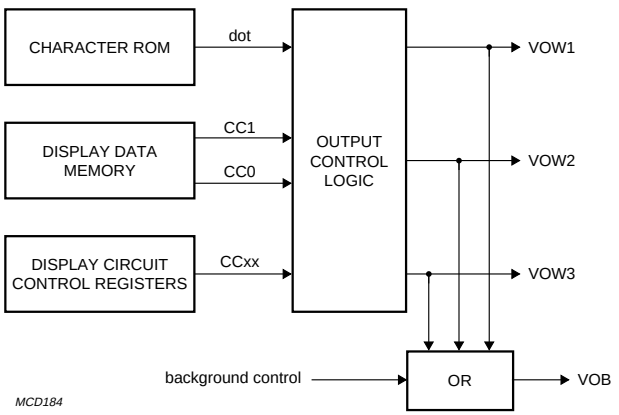


Fig.27 Colour control.

Table 24 Character colour control

COLOUR CODE		CHARACTER OUTPUT PINS1		
CC1	**CC0**	**VOW1 (Red)**	**VOW2 (Green)**	**VOW3 (Blue)**
0	0	CC11	CC21	$\overline{CC11 + CC21}$
0	1	CC12	$\overline{CC12 + CC32}$	CC32
1	0	$\overline{CC23 + CC33}$	CC23	CC33
1	1	CC14	CC24	CC34

Table 25 Possible colour combinations

COLOUR	(CC1, CC0) = (0, 0)			(CC1, CC0) = (0, 1)			(CC1, CC0) = (1, 0)		
	VOW1	**VOW2**	**VOW3**	**VOW1**	**VOW2**	**VOW3**	**VOW1**	**VOW2**	**VOW3**
	CC11	**CC21**	$\overline{CC11+CC21}$	**CC12**	$\overline{CC12+CC32}$	**CC32**	**CC12**	$\overline{CC12+CC32}$	**CC32**
Blue	0	0	1	0	0	1	0	0	1
Green	0	1	0	0	1	0	0	1	0
Red	1	0	0	1	0	0	1	0	0
Yellow	1	1	0	–	–	–	–	–	–
Magenta	–	–	–	1	0	1	–	–	–
Cyan	–	–	–	–	–	–	0	1	1

Table 26 Possible colour combinations (continued)

COLOUR	(CC1, CC0) = (1, 1)		
	VOW1	**VOW2**	**VOW3**
	CC14	**CC24**	**CC34**
Blue	0	0	1
Green	0	1	0
Red	1	0	0
Yellow	1	1	0
Magenta	1	0	1
Cyan	0	1	1
White	1	1	1
Black	0	0	0

12.9 Character ROM

Character ROM contains the dot character fonts.
13 x 8 dots are reserved for each character, regardless of the dot matrix size actually selected.
The dot matrix grid is shown in Fig.28.

Philips provides a software under MS DOS environment (IBM/PC or compatible) to help customer to design the character font on the screen and to generate the bit pattern HEX decimal file automatically.
Contact your local Philips Sales Organization for details.

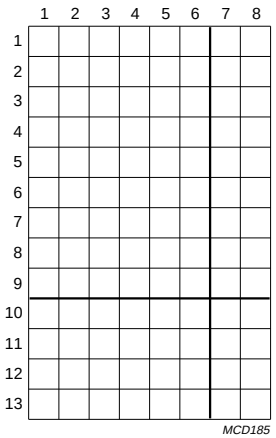


Fig.28 Character ROM.

13 EMULATION MODE

The emulation mode configuration is shown in Fig.29.

In the emulation mode configuration the PCA84C640's CPU is disabled and only its derivative logic is active. The device is controlled by the PCF84C00 bond-out chip. The PCA84C640's two derivative ports act as additional ports for the PCF84C00. The interaction between the two devices is as follows:

1. During the first machine cycle the PCF84C00 fetches an instruction from EPROM and then decodes that instruction.
2. During the second machine cycle the PCF84C00 executes the decoded instruction. If the instruction is related to the derivative ports then DXALE, DXRDN and/or DXWRN become active and the PCA84C640 operates as a peripheral of the PCF84C00.
3. Depending on the type of instruction executed during the second machine cycle the following data transfer happens:
   a) During TS1 data from the EPROM is available on P0.0 to P0.7 which is then available on IB0.0 of the PCF84C00.
   b) During TS4 data from the PCA84C640 can be transferred to the PCF84C00.
   c) During TS6 data from the PCF84C00 can be transferred to the PCA84C640.

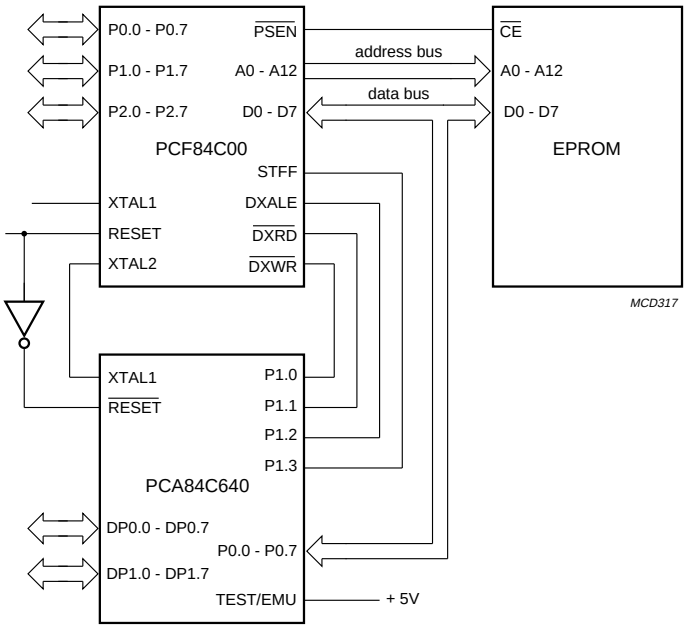


Fig.29 Emulation mode configuration.

14 REGISTER MAP

The number within parentheses denotes the initial state; ‘X’ denotes don’t care.
R = Read, W = Write, R/W =Read/Write.

ADDR	REG	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	R/W
00H	DP0 (pin)	DP0.7 (X)	DP0.6 (X)	DP0.5 (X)	DP0.4 (X)	DP0.3 (X)	DP0.2 (X)	DP0.1 (X)	DP0.0 (X)	R
01H	DP1 (pin)	DP1.7 (X)	DP1.6 (X)	DP1.5 (X)	DP1.4[(1)] (X)	DP1.3 (X)	DP1.2 (X)	DP1.1 (X)	DP1.0 (X)	R
02H	DP0R (latch)	DP0.7 (1)	DP0.6 (1)	DP0.5 (1)	DP0.4 (1)	DP0.3 (1)	DP0.2 (1)	DP0.1 (1)	DP0.0 (1)	R/W
03H	DP1R (latch)	DP1.7 (1)	DP1.6 (1)	DP1.5 (1)	DP1.4[(1)] (1)	DP1.3 (1)	DP1.2 (1)	DP1.1 (1)	DP1.0 (1)	R/W
10H	PWM1	–	–	PWM15 (0)	PWM14 (0)	PWM13 (0)	PWM12 (0)	PWM11 (0)	PWM10 (0)	R/W
11H	PWM2	–	–	PWM25 (0)	PWM24 (0)	PWM23 (0)	PWM22 (0)	PWM21 (0)	PWM20 (0)	R/W
12H	PWM3	–	–	PWM35 (0)	PWM34 (0)	PWM33 (0)	PWM32 (0)	PWM31 (0)	PWM30 (0)	R/W
13H	PWM4	–	–	PWM45 (0)	PWM44 (0)	PWM43 (0)	PWM42 (0)	PWM41 (0)	PWM40 (0)	R/W
14H	PWM5	–	–	PWM55 (0)	PWM54 (0)	PWM53 (0)	PWM52 (0)	PWM51 (0)	PWM50 (0)	R/W
15H	VSTL	–	VST06 (0)	VST05 (0)	VST04 (0)	VST03 (0)	VST02 (0)	VST01 (0)	VST00 (0)	R/W
16H	VSTH	–	VST13 (0)	VST12 (0)	VST11 (0)	VST10 (0)	VST09 (0)	VST08 (0)	VST07 (0)	R/W
17H	AFCO	–	–	–	–	–	AFC2 (0)	AFC1 (0)	AFC0 (0)	R/W
18H	AFCC	–	–	–	–	–	–	–	AFCC (X)	R/W
19H	DP0E/ PWME	SCLE (0)	SDAE (0)	PWM5E (0)	PWM4E (0)	PWM3E (0)	PWM2E (0)	PWM1E (0)	TDACE (0)	R/W
1AH	DP1E/ PWMLVL	–	–	–	AFCE (0)	P14LVL (0)	P6LVL (0)	VOW2E (0)	VOW1E (0)	R/W
20H to 3FH	DATA DISPLAY MEMORY	CC1 (X)	CC0 (X)	MD5 (X)	MD4 (X)	MD3 (X)	MD2 (X)	MD1 (X)	MD0 (X)	W

ADDR	REG	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	R/W
40H	OSDCA	CC34 (0)	CC24 (0)	CC14 (0)	RBLK (0)	ROUND (0)	STBY (1)	VLVL (0)	HLVL (0)	R/W
41H	LINE0A	SZ01 (0)	SZ00 (0)	VP05 (0)	VP04 (0)	VP03 (0)	VP02 (0)	VP01 (0)	VP00 (0)	R/W
42H	LINE0B	BLK0 (0)	VB0 (0)	HP05 (0)	HP04 (0)	HP03 (0)	HP02 (1)	HP01 (0)	HP00 (0)	R/W
43H	OSDCB	CDTV (0)	CDTH (0)	CC33 (0)	CC23 (0)	CC32 (0)	CC12 (1)	CC21 (0)	CCV11 (0)	R/W
44H	LINE1A	SZ11 (0)	SZ10 (0)	VP15 (0)	VP14 (0)	VP13 (0)	VP12 (1)	VP11 (0)	VP10 (0)	R/W
45H	LINE1B	BLK1 (0)	VB1 (0)	HP15 (0)	HP14 (0)	HP13 (0)	HP12 (1)	HP11 (0)	HP10 (0)	R/W

Note

1. These bits are not available in the PCA84C441, PCA84C444, PCA84C641, PCA84C644, PCA84C841 and PCA84C844.

15 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.3	+7.0	V
V_I	input voltage (all inputs)	–0.3	V_{DD} + 0.3	V
I_{OH}	maximum source current for all port lines	–	–10	mA
I_{OL}	maximum sink current for all port lines	–	–30	mA
P_{tot}	total power dissipation	–	900	mW
T_{stg}	storage temperature	–55	+125	°C
T_{amb}	operating ambient temperature (for all devices)	–20	+70	°C

16 DC CHARACTERISTICS

V_{DD} = 4.5 V to 5.5 V; V_{SS} = 0 V; T_{amb} = –20 to +70 °C; all voltages with respect to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	operating supply voltage		4.5	5.0	5.5	V
I_{DD}	operating supply current	f_{OSDCRC} = f_{OSDCLC} = f_{XTAL}; V_{DD} = 5 V; see note 1;				
		f_{XTAL} = 10 MHz	–	5	10	mA
		f_{XTAL} = 6 MHz	–	3.5	8	mA
		f_{OSDCRC} = f_{OSDCLC} = STOP; V_{DD} = 5 V; see note 1;	–			
		f_{XTAL} = 10 MHz	–	3	7	mA
		f_{XTAL} = 6 MHz	–	1.5	3.5	mA
$I_{DD(ID)}$	supply current Idle mode	V_{DD} = 5 V;				
		f_{XTAL} = 10 MHz	–	1.3	3	mA
		f_{XTAL} = 6 MHz; see note 1	–	0.8	1.5	mA
$I_{DD(ST)}$	supply current Stop mode	V_{DD} = 5.5 V; see notes 1 and 2	–	5	10	μA
Inputs						
I_{IH}	HIGH level input current (pin $\overline{RESET}$)	V_{in} = 0.5 V	20	–	–	μA
PORTS P0, P1, DP0, DP1, HSYNCN AND VSYNCN						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
PORTS P0, P1, DP0, DP1, INTN/T0 AND T1						
I_{LI}	input leakage current	$V_{SS} < V_I < V_{DD}$				
	Ports P0, P1, DP0 and DP1		–	–	±10	μA
	Ports INTN/T0 and T1		±0.01	±0.2	±10	μA
Outputs: Ports P0, P1, DP0, DP1; VOB and VOW3 (see Figs 30, 31 and 31)						
I_{OL}	LOW level output sink current					
	Port P0	V_O = 1.2 V	10	–	–	mA
	Ports P1, DP0 and DP1	V_O = 0.4 V	5	10	–	mA
	Ports VOB and VOW3	V_O = 0.4 V	1.2	3	–	mA
PORTS P0, P1, DP0 AND DP1 (see Figs 33 and 33)						
I_{OH}	HIGH level pull-up output source current	V_O = V_{SS}	–	140	400	μA
		V_O = $0.7V_{DD}$	40	100	–	μA
	HIGH level push-pull output source current	V_O = V_{DD} – 0.4 V	3	7	–	mA
OUTPUTS VOB AND VOW3 (see Fig.33)						
I_{OH}	HIGH level push-pull output source current	V_O = V_{DD} – 0.4 V	1.2	3	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AFC characteristics; Port DP1.7/AFC						
V_{AI}	comparator analog input voltage		V_{SS}	–	V_{DD}	V
V_{AE}	conversion error range		–	–	± 0.5	LSB

Notes

1. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; all outputs and sense input lines unloaded. All open drain ports connected to V_{SS}.
2. Crystal is connected between XTAL1 and XTAL2; T1 = V_{SS}; $\overline{INT}$/T0 = V_{DD}.

17 AC CHARACTERISTICS

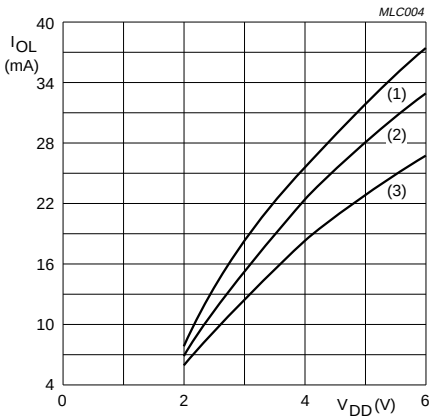
V_{DD} = 5 V; T_{amb} = –20 to +70 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator						
f_{XTAL}	crystal frequency; note 1		1	–	10.0	MHz
$f_{OSC-XTAL}$	oscillator frequency; option 1	g_m = 0.4 mS (typ.)	1	–	6.0	MHz
$f_{OSC-PXE}$			not allowed			MHz
$f_{OSC-XTAL}$	oscillator frequency; option 2	g_m = 1.6 mS (typ.)	4.0	–	10.0	MHz
$f_{OSC-PXE}$			1.0	–	6.0	MHz
$f_{OSC-XTAL}$	oscillator frequency; option 3	g_m = 4.5 mS (typ.)	not allowed			MHz
$f_{OSC-PXE}$			3.0	–	10.0	MHz
C_{XTAL1}	external capacitance at XTAL1					
	with XTAL resonator		not required			pF
	with PXE resonator		–	30	100	pF
C_{XTAL2}	external capacitance at XTAL2					
	with XTAL resonator		not required			pF
	with PXE resonator		–	30	100	pF
f_{DOSC}	on-screen-display clock frequency		4.0	8.0	10.0	MHz

Note

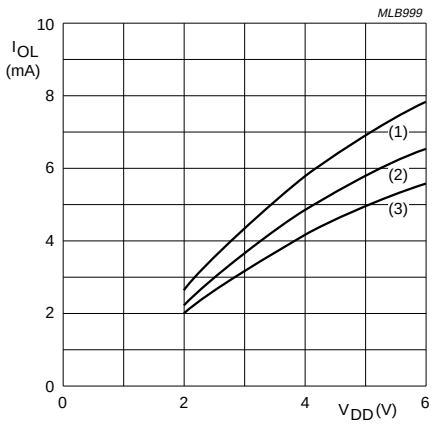
1. Oscillator with three (3) options for optimum use.

17.1 Characteristic curves



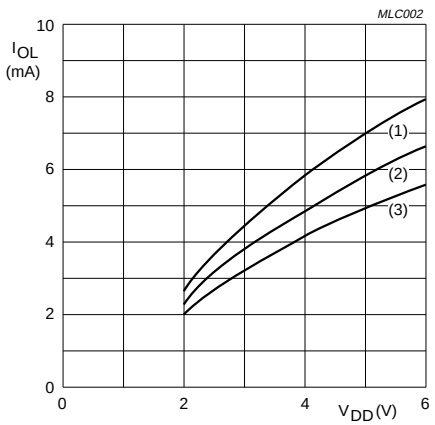
Port P0; V_O = 1.2 V.
(1) T_{amb} = −20°C.
(2) T_{amb} = 25°C.
(3) T_{amb} = 80°C.

Fig.30 Typical LOW level output sink current as a function of the supply voltage.



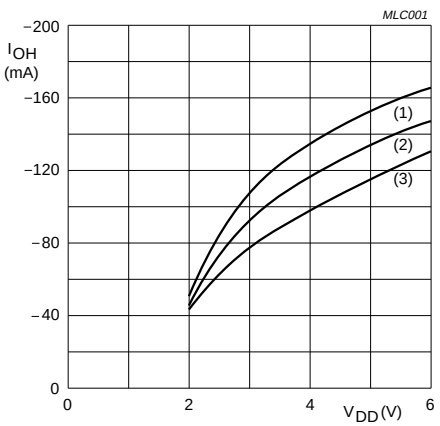
Ports P1, DP0 and DP1; V_O = 0.4 V.
(1) T_{amb} = −20°C.
(2) T_{amb} = 25°C.
(3) T_{amb} = 80°C.

Fig.31 Typical LOW level output sink current as a function of the supply voltage.



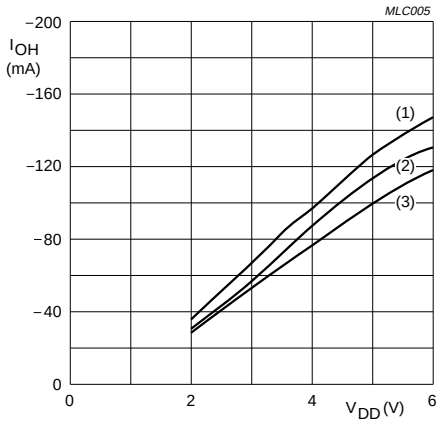
Outputs VOW1, VOW2, VOW3 and VOB; V_O = 0.4 V.
(1) T_{amb} = −20°C.
(2) T_{amb} = 25°C.
(3) T_{amb} = 80°C.

Fig.32 Typical LOW level output sink current as a function of the supply voltage.



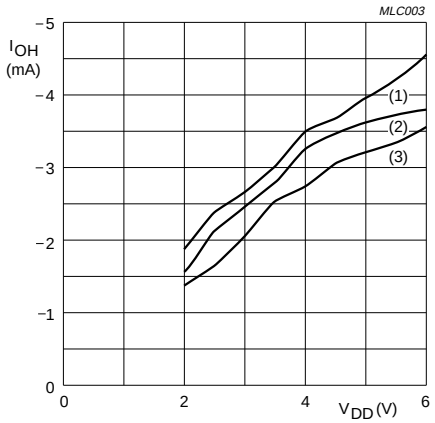
Ports P0, P1, DP0 and DP1; $V_O = V_{SS}$.
(1) T_{amb} = −20°C.
(2) T_{amb} = 25°C.
(3) T_{amb} = 80°C.

Fig.33 Typical HIGH level pull-up output source current as a function of the supply voltage.



Ports P0, P1, DP0 and DP1; $V_O = 0.7V_{DD}$.
(1) $T_{amb} = -20°C$.
(2) $T_{amb} = 25°C$.
(3) $T_{amb} = 80°C$.

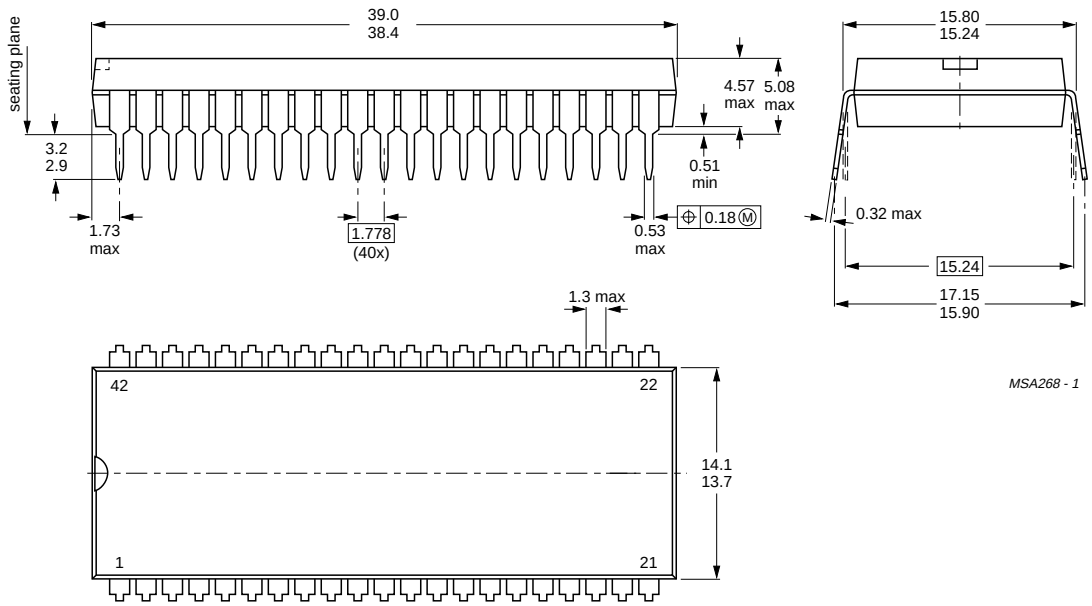
Fig.34 Typical HIGH level pull-up output source current as a function of the supply voltage.



Outputs VOW1, VOW2, VOW3 and VOB; $V_O = V_{DD} - 0.4$ V.
(1) $T_{amb} = -20°C$.
(2) $T_{amb} = 25°C$.
(3) $T_{amb} = 80°C$.

Fig.35 Typical HIGH level pull-up output source current as a function of the supply voltage.

18 PACKAGE OUTLINE



Dimensions in mm.

Fig.36 Plastic shrink dual in-line package; 42 leads (600 mil); SDIP42 (SOT270-1).

19 SOLDERING

19.1 Plastic dual in-line packages

19.1.1 BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

19.1.2 REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

20 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

21 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

22 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.