

### FEATURES

**Ultralow noise (0.1 Hz to 10 Hz)**

**ADR440: 1  $\mu$ V p-p**

**ADR441: 1.2  $\mu$ V p-p**

**ADR443: 1.4  $\mu$ V p-p**

**ADR444: 1.8  $\mu$ V p-p**

**ADR445: 2.25  $\mu$ V p-p**

**Superb temperature coefficient:**

**3 ppm/°C (B Grade)**

**10 ppm/°C (A Grade)**

**Low dropout operation: 500 mV**

**Input range: ( $V_{OUT} + 500$  mV) to 18 V**

**High output current: +10 mA/–5 mA**

**Wide temperature range: –40°C to +125°C**

### APPLICATIONS

**Precision data acquisition systems**

**High resolution data converters**

**Battery-powered instrumentations**

**Portable medical instruments**

**Industrial process control systems**

**Precision instruments**

**Optical control circuits**

### GENERAL DESCRIPTION

The ADR44x series is a family of XFET® voltage references featuring ultralow noise, high accuracy, and low temperature drift performance. Using ADI's patented temperature drift curvature correction and XFET (eXtra implanted junction FET) technology, the ADR44x family's voltage change vs. temperature nonlinearity is greatly minimized.

The XFET references offer better noise performance than buried-Zener references, and XFET references operate off low supply headroom (0.5 V). This combination of features makes the ADR44x family ideally suited for precision signal conversion applications in high-end data acquisition systems, optical networks, and medical requirements.

The ADR44x family has the capability to source up to 10 mA and sink up to 5 mA of output current. It also comes with a TRIM terminal to adjust the output voltage over a 0.5% range without compromising any performance.

### PIN CONFIGURATIONS

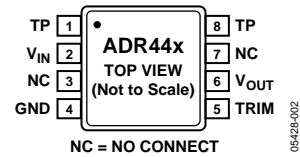


Figure 1. 8-Lead SOIC (R)

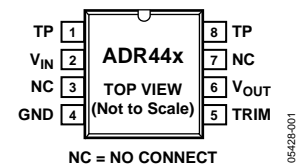


Figure 2. 8-Lead MSOP (RM)

Offered in two electrical grades, the ADR44x family is available in the 8-lead SOIC and MSOP packages. All versions are specified over the extended industrial temperature range (–40°C to +125°C).

**Table 1. Selection Guide**

Model	$V_{OUT}$ (V)	Accuracy (mV)	Temperature Coefficient (ppm/°C)
ADR440B	2.048	$\pm 1$	3
ADR440A	2.048	$\pm 3$	10
ADR441B	2.500	$\pm 1$	3
ADR441A	2.500	$\pm 3$	10
ADR443B	3.000	$\pm 1.2$	3
ADR443A	3.000	$\pm 4$	10
ADR444B	4.096	$\pm 1.6$	3
ADR444A	4.096	$\pm 5$	10
ADR445B	5.000	$\pm 2$	3
ADR445A	5.000	$\pm 6$	10

#### Rev. 0

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## REVISION HISTORY

10/05—Revision 0: Initial Version

## SPECIFICATIONS

### ADR440—ELECTRICAL CHARACTERISTICS

$V_{IN} = 3\text{ V to }18\text{ V}$ ;  $T_A = 25^\circ\text{C}$ ;  $C_{IN}, C_{BYPASS} = 0.1\ \mu\text{F}$ , unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT VOLTAGE						
A Grade	$V_O$		2.045	2.048	2.051	V
B Grade	$V_O$		2.047	2.048	2.049	V
INITIAL ACCURACY						
A Grade	$V_{OERR}$				3	mV
					0.15	%
B Grade	$V_{OERR}$				1	mV
					0.05	%
TEMPERATURE DRIFT						
A Grade SOIC-8	$TC\ V_O$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		2	10	ppm/ $^\circ\text{C}$
MSOP-8	$TC\ V_O$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		2	10	ppm/ $^\circ\text{C}$
B Grade SOIC-8	$TC\ V_O$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1	3	ppm/ $^\circ\text{C}$
LINE REGULATION	$\Delta V_O/\Delta V_{IN}$	$V_{IN} = 3\text{ V to }18\text{ V}, -40^\circ\text{C} < T_A < +125^\circ\text{C}$	-20	+10	+20	ppm/V
LOAD REGULATION						
	$\Delta V_O/\Delta I_{LOAD}$	$I_{LOAD} = 0\text{ mA to }10\text{ mA}, V_{IN} = 3.5\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-50		+50	ppm/mA
	$\Delta V_O/\Delta I_{LOAD}$	$I_{LOAD} = 0\text{ mA to }-5\text{ mA}, V_{IN} = 3.5\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-50		+50	ppm/mA
QUIESCENT CURRENT	$I_{IN}$	No Load, $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		3	3.75	mA
VOLTAGE NOISE	$e_N\text{ p-p}$	0.1 Hz to 10 Hz		1		$\mu\text{V p-p}$
VOLTAGE NOISE DENSITY	$e_N$	1 kHz		60		nV/ $\sqrt{\text{Hz}}$
TURN-ON SETTLING TIME	$t_R$			10		$\mu\text{s}$
LONG-TERM STABILITY <sup>1</sup>	$V_O$	1,000 Hours		50		ppm
OUTPUT VOLTAGE HYSTERESIS	$V_{O\_HYS}$			70		ppm
RIPPLE REJECTION RATION	RRR	$f_{IN} = 10\text{ kHz}$		-75		dB
SHORT CIRCUIT TO GND	$I_{SC}$			27		mA
SUPPLY VOLTAGE OPERATING RANGE	$V_{IN}$		3		18	V
SUPPLY VOLTAGE HEADROOM	$V_{IN} - V_O$		500			mV

<sup>1</sup> The long-term stability specification is noncumulative. This drift in the subsequent 1,000-hour period is significantly lower than in the first 1,000-hour period.

# ADR440/ADR441/ADR443/ADR444/ADR445

## ADR441—ELECTRICAL CHARACTERISTICS

$V_{IN} = 3\text{ V to }18\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT VOLTAGE						
A Grade	$V_O$		2.497	2.5	2.503	V
B Grade	$V_O$		2.499	2.5	2.501	V
INITIAL ACCURACY						
A Grade	$V_{OERR}$				3	mV
					0.12	%
B Grade	$V_{OERR}$				1	mV
					0.04	%
TEMPERATURE DRIFT						
A Grade SOIC-8	$TC V_O$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		2	10	ppm/ $^\circ\text{C}$
MSOP-8	$TC V_O$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		2	10	ppm/ $^\circ\text{C}$
B Grade SOIC-8	$TC V_O$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1	3	ppm/ $^\circ\text{C}$
LINE REGULATION	$\Delta V_O/\Delta V_{IN}$	$V_{IN} = 3\text{ V to }18\text{ V}$ , $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		10	20	ppm/V
LOAD REGULATION	$\Delta V_O/\Delta I_{LOAD}$	$I_{LOAD} = 0\text{ mA to }10\text{ mA}$ , $V_{IN} = 4\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-50		+50	ppm/mA
	$\Delta V_O/\Delta I_{LOAD}$	$I_{LOAD} = 0\text{ mA to }-5\text{ mA}$ , $V_{IN} = 4\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-50		+50	ppm/mA
QUIESCENT CURRENT	$I_{IN}$	No Load, $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		3	3.75	mA
VOLTAGE NOISE	$e_N$ p-p	0.1 Hz to 10 Hz		1.2		$\mu\text{V p-p}$
VOLTAGE NOISE DENSITY	$e_N$	1 kHz		48		nV/ $\sqrt{\text{Hz}}$
TURN-ON SETTLING TIME	$t_R$			10		$\mu\text{s}$
LONG-TERM STABILITY <sup>1</sup>	$V_O$	1,000 Hours		50		ppm
OUTPUT VOLTAGE HYSTERESIS	$V_{O\_HYS}$			70		ppm
RIPPLE REJECTION RATION	RRR	$f_{IN} = 10\text{ kHz}$		-75		dB
SHORT CIRCUIT TO GND	$I_{SC}$			27		mA
SUPPLY VOLTAGE OPERATING RANGE	$V_{IN}$		3		18	V
SUPPLY VOLTAGE HEADROOM	$V_{IN} - V_O$		500			mV

<sup>1</sup> The long-term stability specification is noncumulative. This drift in subsequent 1,000-hour period is significantly lower than in the first 1,000-hour period.

**ADR443—ELECTRICAL CHARACTERISTICS**

$V_{IN} = 3.5\text{ V to }18\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 4.**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT VOLTAGE						
A Grade	$V_O$		2.996	3.0	3.004	V
B Grade	$V_O$		2.9988	3.0	3.0012	V
INITIAL ACCURACY						
A Grade	$V_{OERR}$				4	mV
					0.13	%
B Grade	$V_{OERR}$				1.2	mV
					0.04	%
TEMPERATURE DRIFT						
A Grade SOIC-8	$TC V_O$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		2	10	ppm/ $^\circ\text{C}$
MSOP-8	$TC V_O$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		2	10	ppm/ $^\circ\text{C}$
B Grade SOIC-8	$TC V_O$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1	3	ppm/ $^\circ\text{C}$
LINE REGULATION	$\Delta V_O/\Delta V_{IN}$	$V_{IN} = 3.5\text{ V to }18\text{ V}$ , $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		10	20	ppm/V
LOAD REGULATION	$\Delta V_O/\Delta I_{LOAD}$	$I_{LOAD} = 0\text{ mA to }10\text{ mA}$ , $V_{IN} = 5\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-50		+50	ppm/mA
	$\Delta V_O/\Delta I_{LOAD}$	$I_{LOAD} = 0\text{ mA to }-5\text{ mA}$ , $V_{IN} = 5\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-50		+50	ppm/mA
QUIESCENT CURRENT	$I_{IN}$	No Load, $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		3	3.75	mA
VOLTAGE NOISE	$e_N$ p-p	0.1 Hz to 10 Hz		1.4		$\mu\text{V p-p}$
VOLTAGE NOISE DENSITY	$e_N$	1 kHz		64		$\text{nV}/\sqrt{\text{Hz}}$
TURN-ON SETTLING TIME	$t_R$			10		$\mu\text{s}$
LONG-TERM STABILITY <sup>1</sup>	$V_O$	1,000 Hours		50		ppm
OUTPUT VOLTAGE HYSTERESIS	$V_{O\_HYS}$			70		ppm
RIPPLE REJECTION RATION	RRR	$f_{IN} = 10\text{ kHz}$		-75		dB
SHORT CIRCUIT TO GND	$I_{SC}$			27		mA
SUPPLY VOLTAGE OPERATING RANGE	$V_{IN}$		3.5		18	V
SUPPLY VOLTAGE HEADROOM	$V_{IN} - V_O$		500			mV

<sup>1</sup> The long-term stability specification is noncumulative. This drift in the subsequent 1,000-hour period is significantly lower than in the first 1,000-hour period.

# ADR440/ADR441/ADR443/ADR444/ADR445

## ADR444—ELECTRICAL CHARACTERISTICS

$V_{IN} = 4.6\text{ V to }18\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 5.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT VOLTAGE						
A Grade	$V_O$		4.091	4.096	4.101	V
B Grade	$V_O$		4.0944	4.096	4.0976	V
INITIAL ACCURACY						
A Grade	$V_{OERR}$				5	mV
					0.13	%
B Grade	$V_{OERR}$				1.6	mV
					0.04	%
TEMPERATURE DRIFT						
A Grade SOIC-8	$TC V_O$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		2	10	ppm/ $^\circ\text{C}$
MSOP-8	$TC V_O$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		2	10	ppm/ $^\circ\text{C}$
B Grade SOIC-8	$TC V_O$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1	3	ppm/ $^\circ\text{C}$
LINE REGULATION	$\Delta V_O/\Delta V_{IN}$	$V_{IN} = 4.6\text{ V to }18\text{ V}$ , $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		10	20	ppm/V
LOAD REGULATION	$\Delta V_O/\Delta I_{LOAD}$	$I_{LOAD} = 0\text{ mA to }10\text{ mA}$ , $V_{IN} = 5.5\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-50		+50	ppm/mA
	$\Delta V_O/\Delta I_{LOAD}$	$I_{LOAD} = 0\text{ mA to }-5\text{ mA}$ , $V_{IN} = 5.5\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-50		+50	ppm/mA
QUIESCENT CURRENT	$I_{IN}$	No Load, $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		3	3.75	mA
VOLTAGE NOISE	$e_n$ p-p	0.1 Hz to 10 Hz		1.8		$\mu\text{V p-p}$
VOLTAGE NOISE DENSITY	$e_n$	1 kHz		64		$\text{nV}/\sqrt{\text{Hz}}$
TURN-ON SETTLING TIME	$t_R$			10		$\mu\text{s}$
LONG-TERM STABILITY <sup>1</sup>	$V_O$	1,000 Hours		50		ppm
OUTPUT VOLTAGE HYSTERISIS	$V_{O\_HYS}$			70		ppm
RIPPLE REJECTION RATION	RRR	$f_{IN} = 10\text{ kHz}$		-75		dB
SHORT CIRCUIT TO GND	$I_{SC}$			27		mA
SUPPLY VOLTAGE OPERATING RANGE	$V_{IN}$		4.6		18	V
SUPPLY VOLTAGE HEADROOM	$V_{IN} - V_O$		500			mV

<sup>1</sup> The long-term stability specification is noncumulative. This drift in the subsequent 1,000-hour period is significantly lower than in the first 1,000-hour period.

**ADR445—ELECTRICAL CHARACTERISTICS**

V<sub>IN</sub> = 5.5 V to 18 V, T<sub>A</sub> = 25°C unless otherwise noted.

**Table 6.**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT VOLTAGE						
A Grade	V <sub>O</sub>		4.994	5.000	5.006	V
B Grade	V <sub>O</sub>		4.998	5.000	5.002	V
INITIAL ACCURACY						
A Grade	V <sub>OERR</sub>				6	mV
					0.12	%
B Grade	V <sub>OERR</sub>				2	mV
					0.04	%
TEMPERATURE DRIFT						
A Grade SOIC-8	TC V <sub>O</sub>	-40°C < T <sub>A</sub> < +125°C		2	10	ppm/°C
MSOP-8	TC V <sub>O</sub>	-40°C < T <sub>A</sub> < +125°C		2	10	ppm/°C
B Grade SOIC-8	TC V <sub>O</sub>	-40°C < T <sub>A</sub> < +125°C		1	3	ppm/°C
LINE REGULATION	ΔV <sub>O</sub> /ΔV <sub>IN</sub>	V <sub>IN</sub> = 5.5 V to 18 V, -40°C < T <sub>A</sub> < +125°C		10	20	ppm/V
LOAD REGULATION	ΔV <sub>O</sub> /ΔI <sub>LOAD</sub>	I <sub>LOAD</sub> = 0 mA to 10 mA, V <sub>IN</sub> = 6.5 V -40°C < T <sub>A</sub> < +125°C	-50		+50	ppm/mA
	ΔV <sub>O</sub> /ΔI <sub>LOAD</sub>	I <sub>LOAD</sub> = 0 mA to -5 mA, V <sub>IN</sub> = 6.5 V -40°C < T <sub>A</sub> < +125°C	-50		+50	ppm/mA
QUIESCENT CURRENT	I <sub>IN</sub>	No Load, -40°C < T <sub>A</sub> < +125°C		3	3.75	mA
VOLTAGE NOISE	e <sub>N</sub> p-p	0.1 Hz to 10 Hz		2.25		μV p-p
VOLTAGE NOISE DENSITY	e <sub>N</sub>	1 kHz		64		nV/√Hz
TURN-ON SETTLING TIME	t <sub>R</sub>			10		μs
LONG-TERM STABILITY <sup>1</sup>	V <sub>O</sub>	1,000 Hours		50		ppm
OUTPUT VOLTAGE HYSTERESIS	V <sub>O_HYS</sub>			70		ppm
RIPPLE REJECTION RATION	RRR	f <sub>IN</sub> = 10 kHz		-75		dB
SHORT CIRCUIT TO GND	I <sub>SC</sub>			27		mA
SUPPLY VOLTAGE OPERATING RANGE	V <sub>IN</sub>		5.5		18	V
SUPPLY VOLTAGE HEADROOM	V <sub>IN</sub> - V <sub>O</sub>		500			mV

<sup>1</sup> The long-term stability specification is noncumulative. This drift in the subsequent 1,000-hour period is significantly lower than in the first 1,000-hour period.

# ADR440/ADR441/ADR443/ADR444/ADR445

## ABSOLUTE MAXIMUM RATINGS

At 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
Supply Voltage	20 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range R, RM Packages	-65°C to +125°C
Operating Temperature Range	-40°C to +125°C
Junction Temperature Range	-65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## PACKAGE TYPE

Table 8.

Package Type	$\theta_{JA}$ <sup>1</sup>	$\theta_{JC}$	Unit
8-Lead SOIC (R)	130	43	°C/W
8-Lead MSOP (RM)	190		°C/W

<sup>1</sup>  $\theta_{JA}$  is specified for worst-case conditions (device soldered in circuit board for surface mount packages). Contact sales for the latest information of release dates.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.





## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 7V$ ,  $T_A = 25^\circ C$ ;  $C_{IN}$ ,  $C_{BYPASS} = 0.1 \mu F$ ; unless otherwise noted.

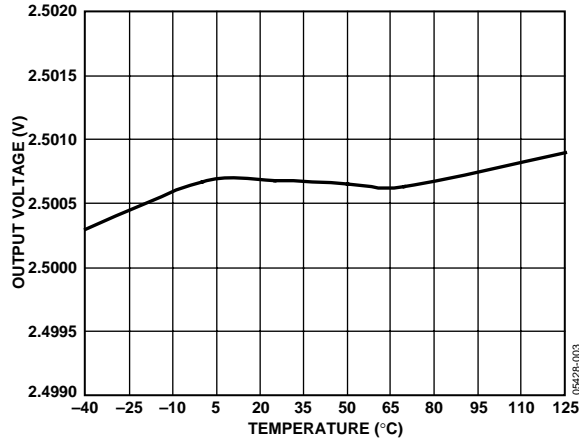


Figure 3. ADR441  $V_{OUT}$  vs. Temperature

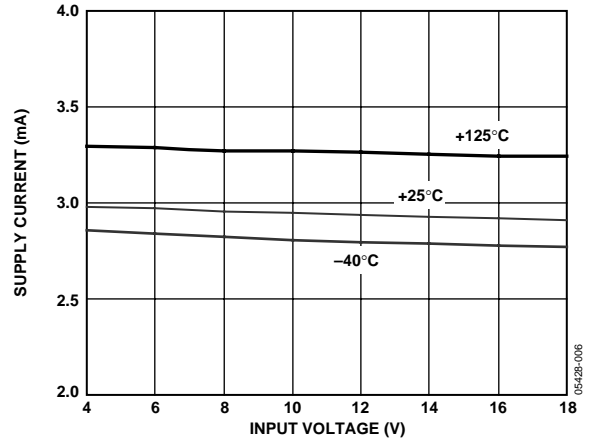


Figure 6. ADR441 Supply Current vs. Input Voltage

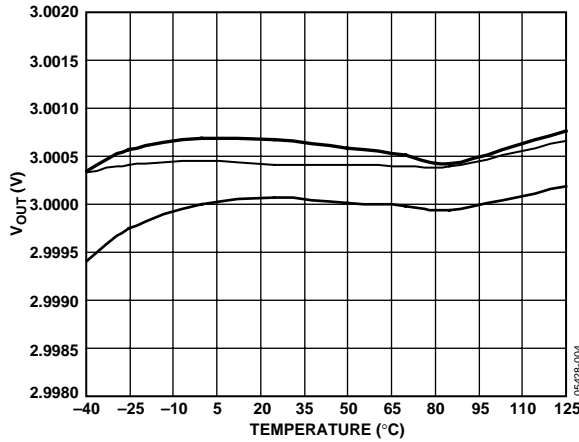


Figure 4. ADR444  $V_{OUT}$  vs. Temperature

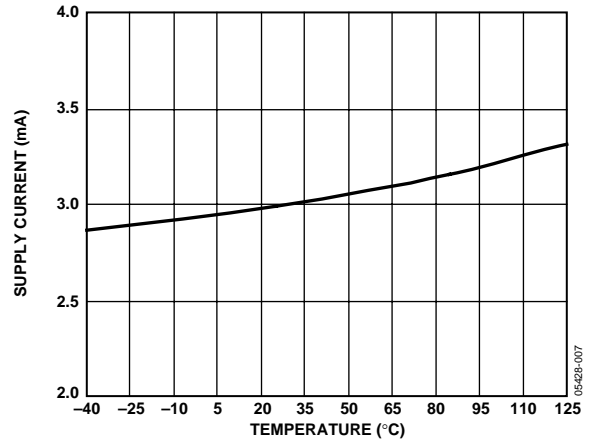


Figure 7. ADR441 Supply Current vs. Temperature

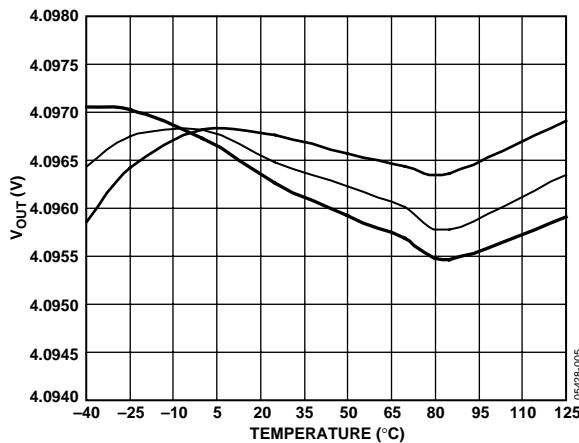


Figure 5. ADR445  $V_{OUT}$  vs. Temperature

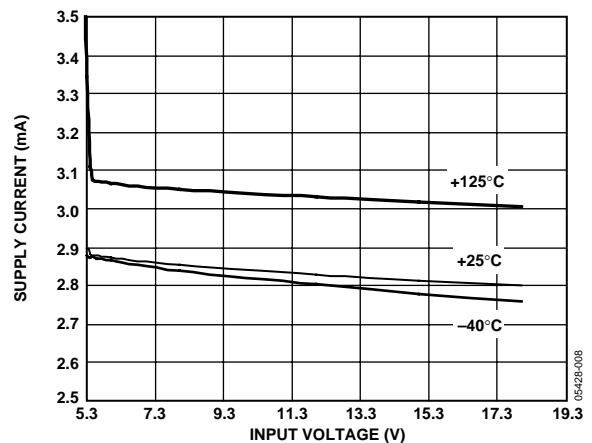


Figure 8. ADR445 Supply Current vs. Input Voltage

# ADR440/ADR441/ADR443/ADR444/ADR445

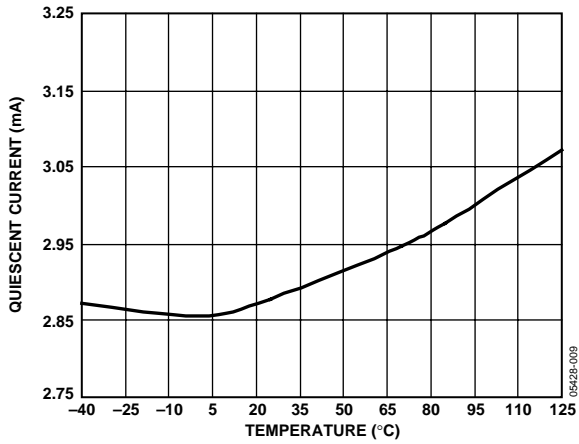


Figure 9. ADR445 Quiescent Current vs. Temperature

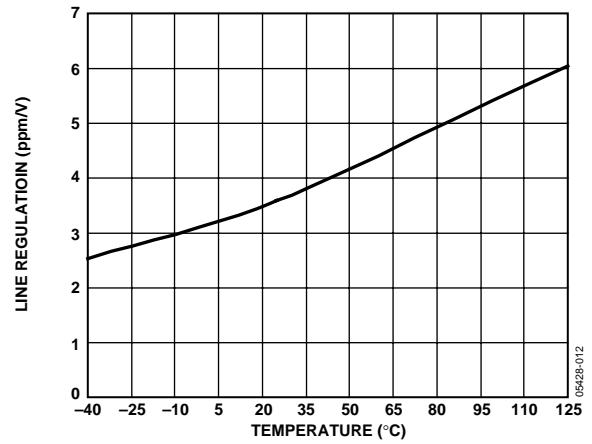


Figure 12. ADR445 Line Regulation vs. Temperature

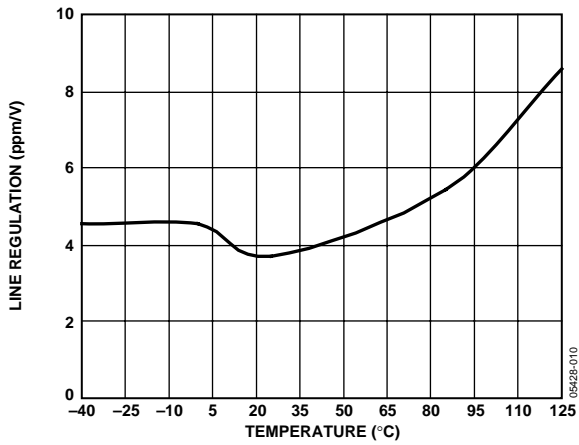


Figure 10. ADR441 Line Regulation vs. Temperature

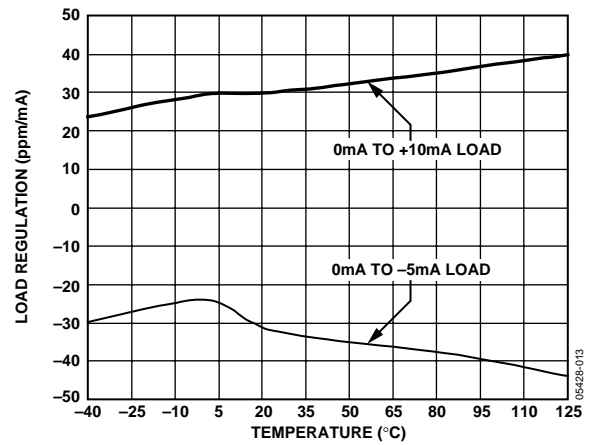


Figure 13. ADR445 Load Regulation vs. Temperature

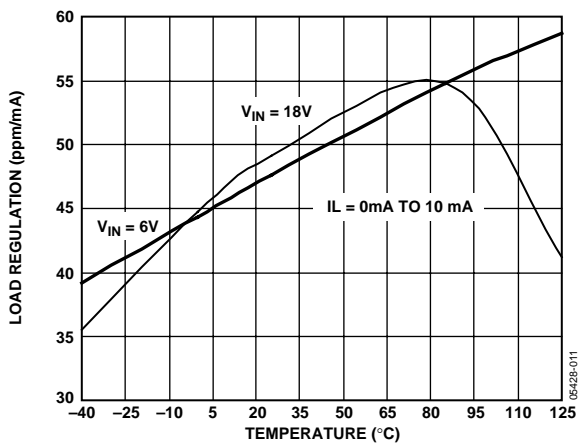


Figure 11. ADR441 Load Regulation vs. Temperature

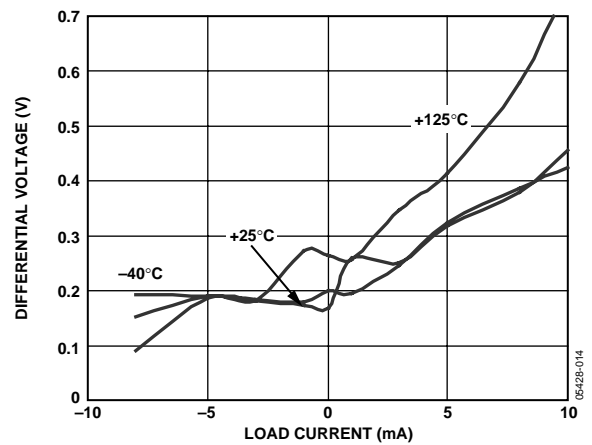


Figure 14. ADR441 Minimum Input/Output Differential Voltage vs. Load Current

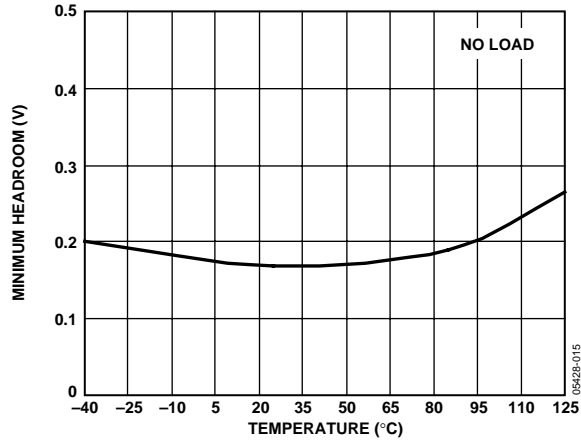


Figure 15. ADR441 Minimum Headroom vs. Temperature

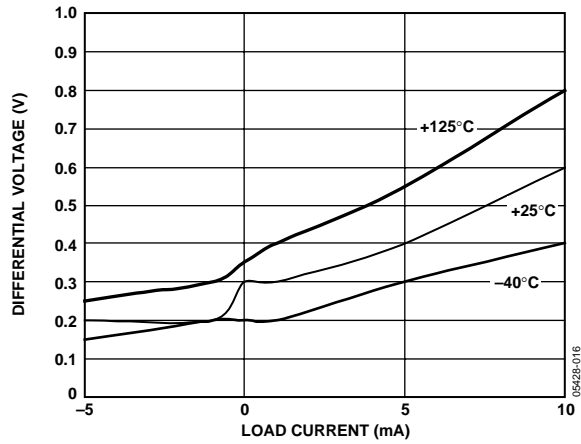


Figure 16. ADR445 Minimum Input/Output Differential Voltage vs. Load Current

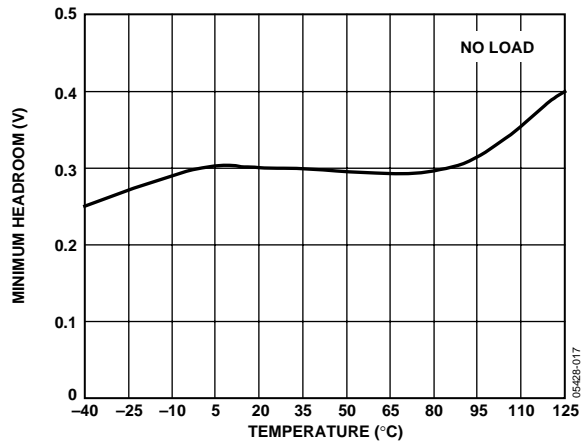


Figure 17. ADR445 Minimum Headroom vs. Temperature

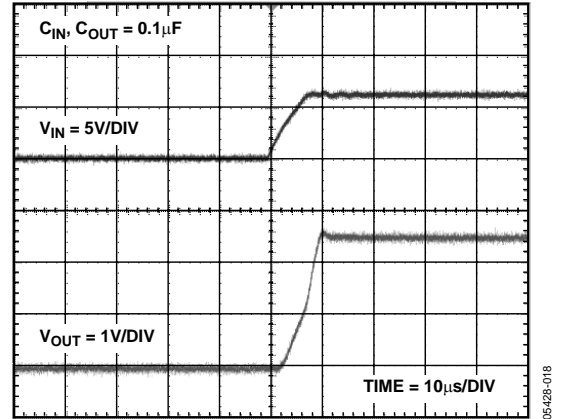


Figure 18. ADR441 Turn-On Response

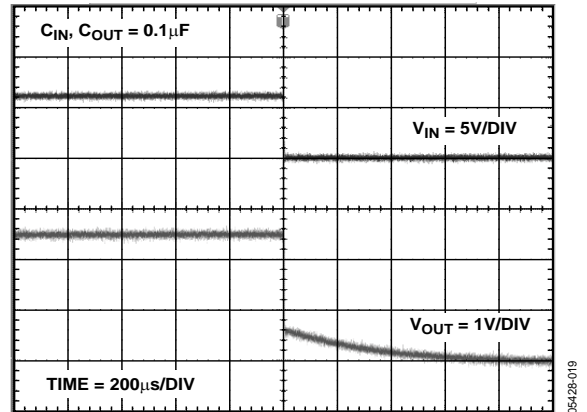


Figure 19. ADR441 Turn-Off Response

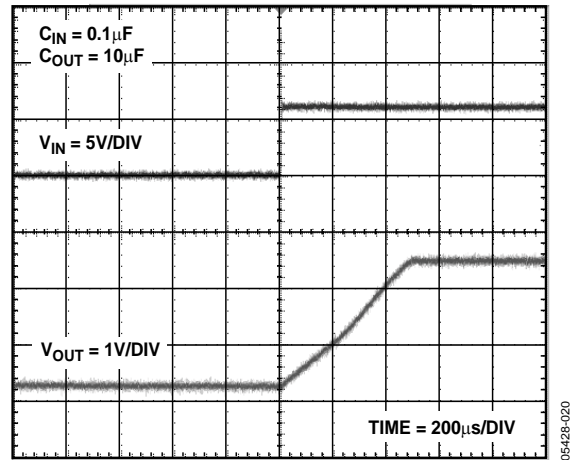


Figure 20. ADR441 Turn-On Response

# ADR440/ADR441/ADR443/ADR444/ADR445

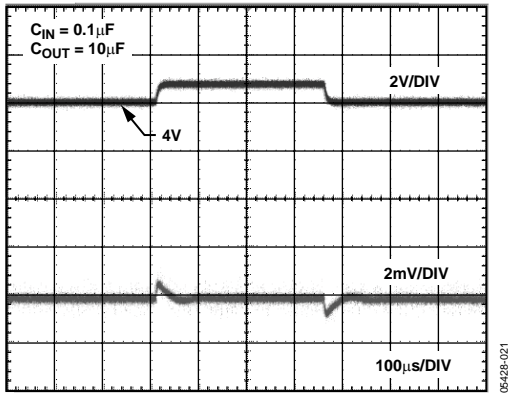


Figure 21. ADR441 Line Transient Response

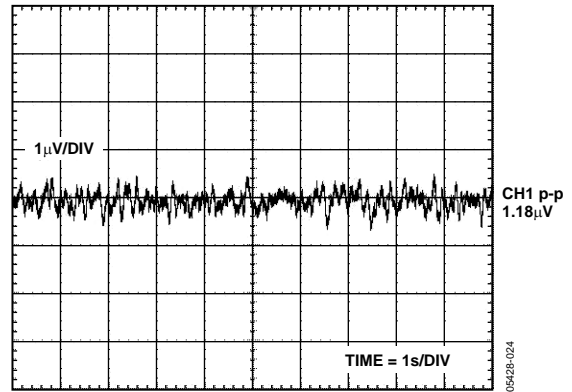


Figure 24. ADR441 0.1 Hz to 10.0 Hz Voltage Noise

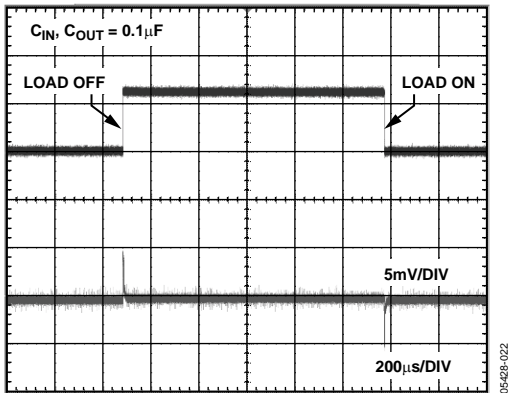


Figure 22. ADR441 Load Transient Response

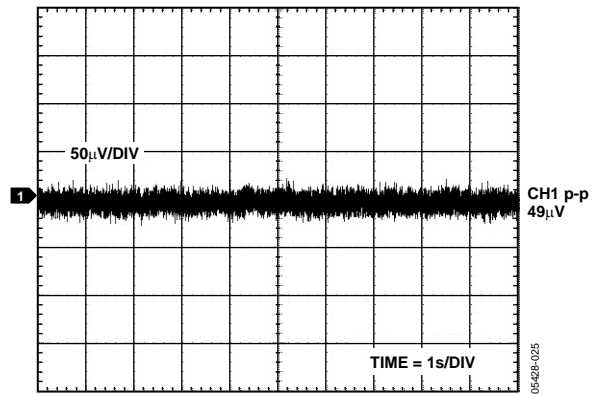


Figure 25. ADR441 10 Hz to 10 kHz Voltage Noise

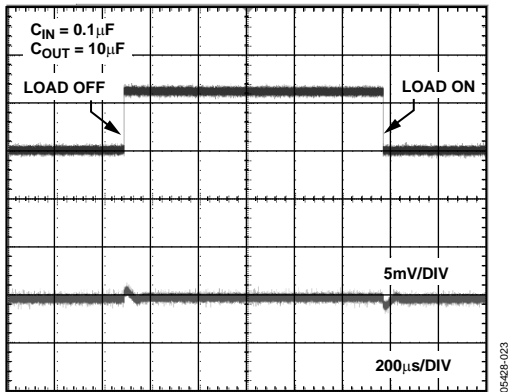


Figure 23. ADR441 Load Transient Response

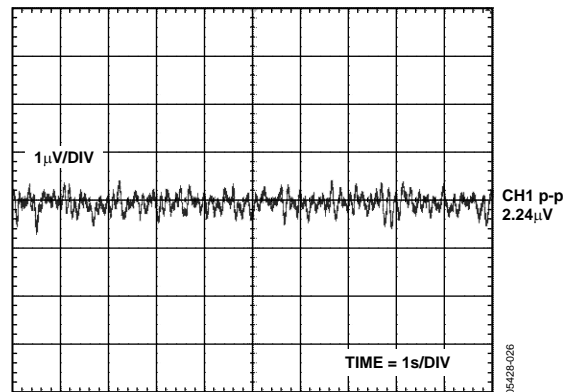


Figure 26. ADR445 0.1 Hz to 10.0 Hz Voltage Noise

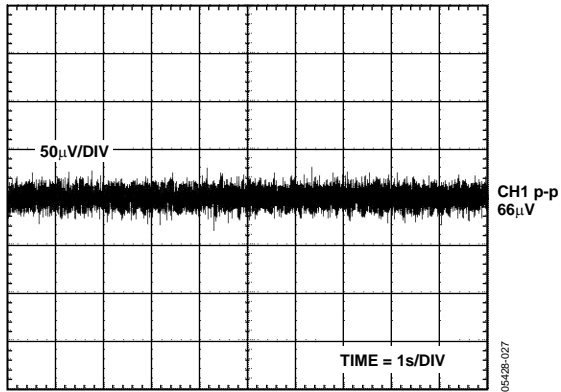


Figure 27. ADR445 10 Hz to 10 kHz Voltage Noise

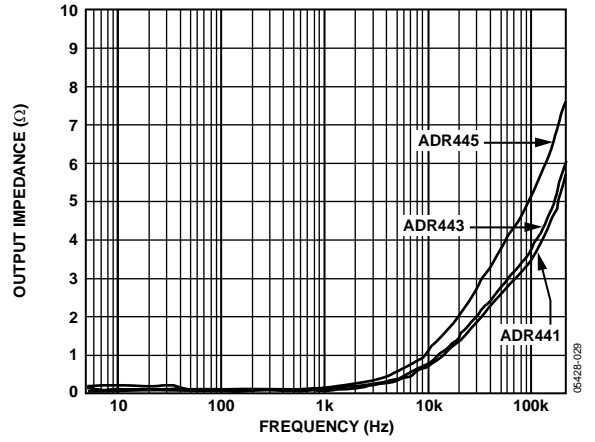


Figure 29. Output Impedance vs. Frequency

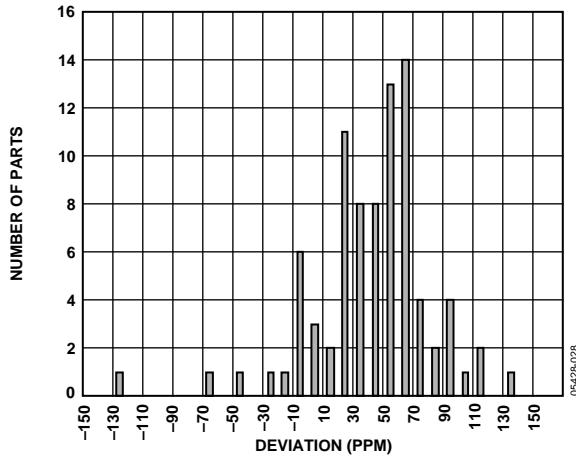


Figure 28. ADR441 Typical Hysteresis

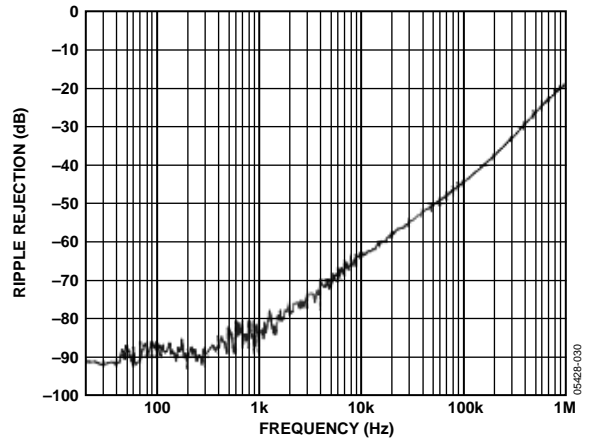


Figure 30. Ripple Rejection vs. Frequency

# ADR440/ADR441/ADR443/ADR444/ADR445

## THEORY OF OPERATION

The ADR44x series of references uses a new reference generation technique known as XFET (eXtra implanted junction FET). This technique yields a reference with low dropout, good thermal hysteresis, and exceptionally low noise. The core of the XFET reference consists of two junction field-effect transistors (JFETs), one of which has an extra channel implant to raise its pinch-off voltage. By running the two JFETs at the same drain current, the difference in pinch-off voltage can be amplified and used to form a highly stable voltage reference.

The intrinsic reference voltage is around 0.5 V with a negative temperature coefficient of about  $-120 \text{ ppm}/^\circ\text{C}$ . This slope is essentially constant to the dielectric constant of silicon and can be closely compensated for by adding a correction term generated in the same fashion as the proportional-to-temperature (PTAT) term used to compensate band gap references. The advantage of an XFET reference is the correction term is approximately 20 times lower and requires less correction than a band gap reference. This results in much lower noise, because most of the noise of a band gap reference results from the temperature compensation circuitry.

Figure 31 shows the basic topology of the ADR44x series. The temperature correction term is provided by a current source with a value designed to be proportional to absolute temperature. The general equation is

$$V_{OUT} = G \times (\Delta V_P - R1 \times I_{PTAT}) \quad (1)$$

where:

$G$  is the gain of the reciprocal of the divider ratio.  
 $\Delta V_P$  is the difference in pinch-off voltage between the two JFETs.  
 $I_{PTAT}$  is the positive temperature coefficient correction current.

ADR44x devices are created by on-chip adjustment of  $R2$  and  $R3$  to achieve the different voltage option at the reference output.

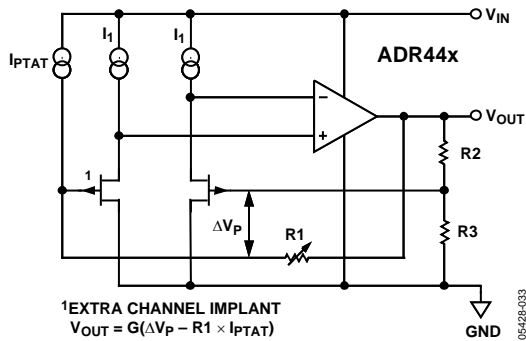


Figure 31. Simplified Schematic Device

## POWER DISSIPATION CONSIDERATIONS

The ADR44x family of references is guaranteed to deliver load currents to 10 mA with an input voltage that ranges from 2.6 V to 18 V. When these devices are used in applications at higher currents, users should use the following equation to account for the temperature effects due to the power dissipation increases.

$$T_J = P_D \times \theta_{JA} + T_A \quad (2)$$

where:

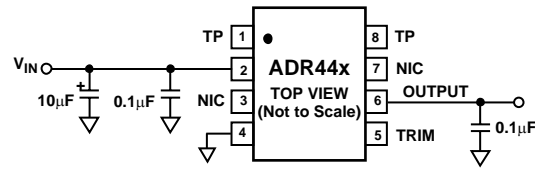
$T_J$  and  $T_A$  are the junction and ambient temperatures.

$P_D$  is the device power dissipation.

$\theta_{JA}$  is the device package thermal resistance.

## BASIC VOLTAGE REFERENCE CONNECTIONS

The ADR44x family requires a  $0.1 \mu\text{F}$  capacitor on the input and output for stability. While not required for operation, a  $10 \mu\text{F}$  capacitor at the input can help with line voltage transient performance.



- NOTES  
 1. NIC = NO INTERNAL CONNECTION  
 2. TP = TEST PIN (DO NOT CONNECT)

Figure 32. Basic Voltage Reference Configuration

## NOISE PERFORMANCE

The noise generated by the ADR44x family of references is typically less than  $1.4 \mu\text{V p-p}$  over the 0.1 Hz to 10.0 Hz band for ADR440, ADR441, and ADR443. Figure 24 shows the 0.1 Hz to 10 Hz noise of the ADR441, which is only  $1.2 \mu\text{V p-p}$ . The noise measurement is made with a band-pass filter made of a 2-pole high-pass filter with a corner frequency at 0.1 Hz and a 2-pole low-pass filter with a corner frequency at 10.0 Hz.

## TURN-ON TIME

Upon application of power (cold start), the time required for the output voltage to reach its final value within a specified error band is defined as the turn-on settling time. Two components normally associated with this are the time for the active circuits to settle, and the time for the thermal gradients on the chip to stabilize. Figure 18 and Figure 19 show the turn-on and turn-off settling times for the ADR441.

## APPLICATIONS

### OUTPUT ADJUSTMENT

The ADR44x family features a TRIM pin that allows the user to adjust the output voltage of the part over a limited range. This allows both errors from the reference and overall system errors to be trimmed out by connecting a potentiometer between the output and ground, with the wiper connected to the TRIM pin. Figure 33 shows the optimal trim configuration. R1 allows fine adjustment of the output and is not always required. R<sub>P</sub> should be sufficiently large so that the maximum output current from the ADR44x is not exceeded.

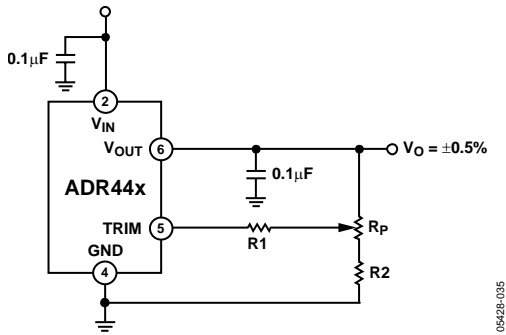


Figure 33. ADR44x Trim Function

Using the trim function had a negligible effect on the temperature performance of the ADR44x family. However, all resistors used need to be low temperature coefficient resistors, or errors can occur.

### BIPOLAR OUTPUTS

By connecting the output of the ADR44x to the inverting terminal of an op amp, it is possible to obtain both positive and negative reference voltages. Care must be taken when choosing Resistor R1 and Resistor R2 (see Figure 34). They must be matched as closely as possible to ensure minimal differences between the negative and positive outputs. In addition, care must be taken to ensure performance over temperature. Use low temperature coefficient resistors if the circuit is to be used over temperature; otherwise, differences will exist between the two outputs.

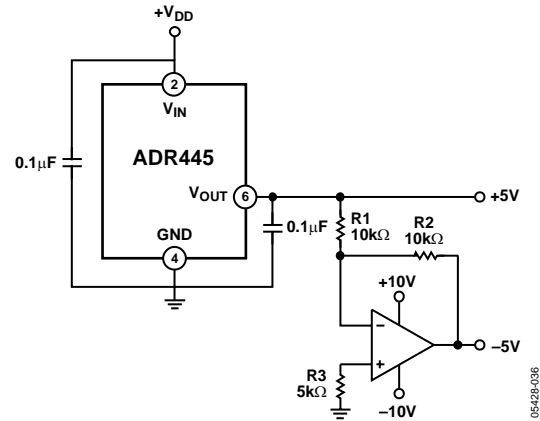


Figure 34. ADR 44x Bipolar Outputs

### NEGATIVE REFERENCE

Figure 35 shows how to connect the ADR44x and a standard op amp, such as the OP1177, to provide negative voltage. This configuration provides two main advantages: First, it only requires two devices; therefore, it does not require excessive board space. Second, and more importantly, it does not require any external resistors. This means the performance of this circuit does not rely on choosing low TC resistors to ensure accuracy.

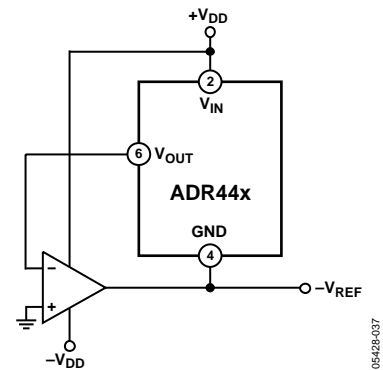


Figure 35. Negative Reference

V<sub>OUT</sub> is at virtual ground, and the negative reference is taken directly from the output of the op amp. If the negative supply voltage is close to the reference output, the op amp must be dual supply and have low offset and rail-to-rail capability.

# ADR440/ADR441/ADR443/ADR444/ADR445

## PROGRAMMABLE VOLTAGE SOURCE

To obtain different voltages than those offered by the ADR44x, some extra components are needed. In Figure 36, two potentiometers are used to set the desired voltage, while the buffering amplifier provides current drive. The potentiometer connected between  $V_{OUT}$  and ground, with its wiper connected to the noninverting input of the op amp, takes care of coarse trim. The second potentiometer, with its wiper connected to the trim terminal of the ADR44x, is used for fine adjustment. Resolution depends on the end-to-end resistance value and the resolution of the selected potentiometer.

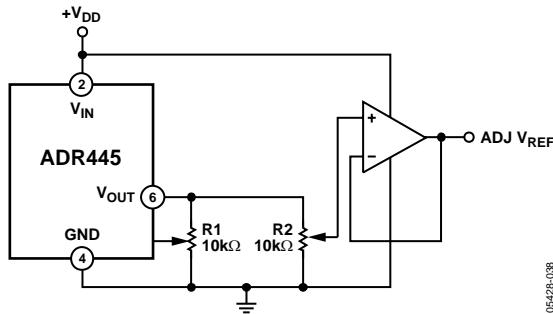


Figure 36. Programmable Voltage Source

For a completely programmable solution, replace the two potentiometers in Figure 36 with one of ADI's dual digital potentiometers, which offer either SPI® or I<sup>2</sup>C interfaces. These interfaces set the position of the wiper on both potentiometers and allow the output voltage to be set. Table 9 lists compatible ADI digital potentiometers.

Table 9. Digital Potentiometer Parts

Part No.	No. Chan	No. Pos	ITF	R (kΩ)	VDD <sup>1</sup>
AD5251	2.00	64.00	I <sup>2</sup> C	1, 10, 50, 100	5.5
AD5207	2.00	256.00	SPI	10, 50, 100	5.5
AD5242	2.00	256.00	I <sup>2</sup> C	10, 100, 1M	5.5
AD5262	2.00	256.00	SPI	20, 50, 200	15
AD5282	2.00	256.00	I <sup>2</sup> C	20, 50, 100	15
AD5252	2.00	256.00	I <sup>2</sup> C	1, 10, 50, 200	5.5
AD5232	2.00	256.00	SPI	10, 50, 100	5.5
AD5235	2.00	1024.00	SPI	25, 250	5.5
ADN2850	2.00	1024.00	SPI	25, 250	5.5

<sup>1</sup> Can also use a negative supply.

By adding a negative supply to the op amp, it is possible for the user to also produce a negative programmable reference by connecting the reference output to the inverting terminal of the op amp. Choose feedback resistors to minimize errors over temperature.

## PROGRAMMABLE CURRENT SOURCE

It is possible to build a programmable current source using a similar setup as the programmable voltage source, as shown in Figure 37. The constant voltage on the gate of the transistor sets the current through the load. Varying the voltage on the gate changes the current. This circuit does not require a dual digital potentiometer.

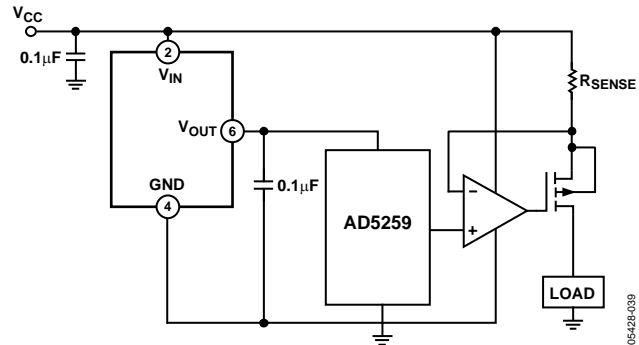


Figure 37. Programmable Current Source

## HIGH VOLTAGE FLOATING CURRENT SOURCE

Use the circuit in Figure 38 to generate a floating current source with minimal self-heating. This particular configuration can operate on high supply voltages determined by the breakdown voltage of the N-channel JFET.

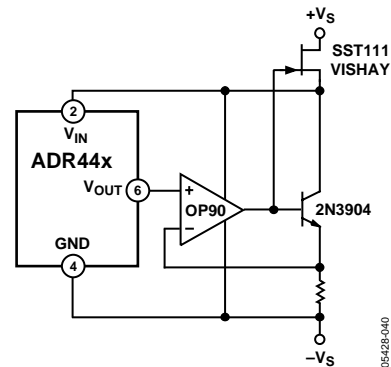


Figure 38. Floating Current Source



**PRECISION OUTPUT REGULATOR (BOOSTED REFERENCE)**

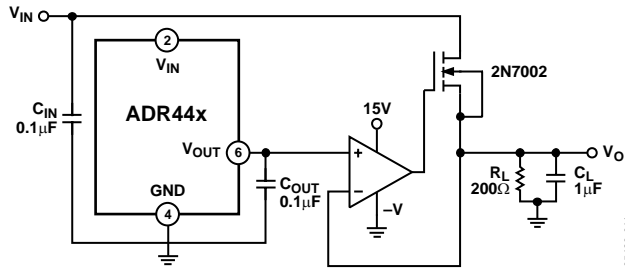
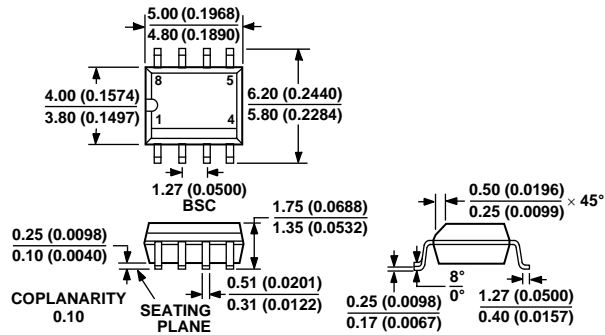


Figure 39. Boosted Output Reference

Higher current drive capability without sacrificing accuracy can be obtained using the circuit in Figure 39. The op amp regulates the MOSFET turn-on, which forces  $V_O$  to equal the  $V_{REF}$ . Current is then drawn from  $V_{IN}$ , which allows increased current drive capability. The circuit allows a 50 mA load; if higher current drive is required, use a larger MOSFET. For fast transient response, add a buffer at  $V_O$  to aid with capacitive loading.

# ADR440/ADR441/ADR443/ADR444/ADR445

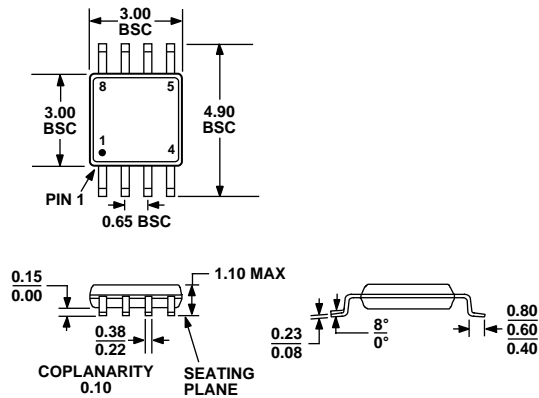
## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 40. 8-Lead Standard Small Outline Package [SOIC\_N]  
Narrow Body  
(R-8)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 41. 8-Lead Mini Small Outline Package [MSOP]  
(RM-8)

Dimensions show in millimeters

# ADR440/ADR441/ADR443/ADR444/ADR445

## ORDERING GUIDE

Model	Output Voltage	Initial Accuracy		Temperature Coefficient Package	Package Description	Branding	Temperature Range (°C)	Ordering Quantity
	(V <sub>O</sub> ) V	(mV)	(%)	(ppm/°C)				
ADR440ARZ <sup>1</sup>	2.048	3	0.15	10	8-lead SOIC_N		-40 to +125	98
ADR440ARZ-REEL7 <sup>1</sup>	2.048	3	0.15	10	8-Lead SOIC_N		-40 to +125	1,000
ADR440ARMZ <sup>1</sup>	2.048	3	0.15	10	8-Lead MSOP	R01	-40 to +125	98
ADR440ARMZ-REEL7 <sup>1</sup>	2.048	3	0.15	10	8-Lead MSOP	R01	-40 to +125	1,000
ADR440BRZ <sup>1</sup>	2.048	1	0.05	3	8-lead SOIC_N		-40 to +125	98
ADR440BRZ-REEL7 <sup>1</sup>	2.048	1	0.05	3	8-Lead SOIC_N		-40 to +125	1,000
ADR441ARZ <sup>1</sup>	2.500	3	0.12	10	8-Lead SOIC_N		-40 to +125	98
ADR441ARZ-REEL7 <sup>1</sup>	2.500	3	0.12	10	8-Lead SOIC_N		-40 to +125	1,000
ADR441ARMZ <sup>1</sup>	2.500	3	0.12	10	8-Lead MSOP	R02	-40 to +125	98
ADR441ARMZ-REEL7 <sup>1</sup>	2.500	3	0.12	10	8-Lead MSOP	R02	-40 to +125	1,000
ADR441BRZ <sup>1</sup>	2.500	1	0.04	3	8-Lead SOIC_N		-40 to +125	98
ADR441BRZ-REEL7 <sup>1</sup>	2.500	1	0.04	3	8-Lead SOIC_N		-40 to +125	1,000
ADR443ARZ <sup>1</sup>	3.000	4	0.12	10	8-Lead SOIC_N		-40 to +125	98
ADR443ARZ-REEL7 <sup>1</sup>	3.000	4	0.12	10	8-Lead SOIC_N		-40 to +125	1,000
ADR443ARMZ <sup>1</sup>	3.000	4	0.12	10	8-Lead MSOP	R03	-40 to +125	98
ADR443ARMZ-REEL7 <sup>1</sup>	3.000	4	0.12	10	8-Lead MSOP	R03	-40°C to +125°C	1,000
ADR443BRZ <sup>1</sup>	3.000	1.2	0.05	3F	8-Lead SOIC_N		-40 to +125	98
ADR443BRZ-REEL7 <sup>1</sup>	3.000	1.2	0.05	3	8-Lead SOIC_N		-40 to +125	1,000
ADR444ARZ <sup>1</sup>	4.096	5	0.13	10	8-Lead SOIC_N		-40 to +125	98
ADR444ARZ-REEL7 <sup>1</sup>	4.096	5	0.13	10	8-Lead SOIC_N		-40 to +125	1,000
ADR444ARMZ <sup>1</sup>	4.096	5	0.13	10	8-Lead MSOP	R04	-40 to +125	98
ADR444ARMZ-REEL7 <sup>1</sup>	4.096	5	0.13	10	8-Lead MSOP	R04	-40 to +125	1,000
ADR444BRZ <sup>1</sup>	4.096	1.6	0.04	3	8-Lead SOIC_N		-40 to +125	98
ADR444BRZ-REEL7 <sup>1</sup>	4.096	1.6	0.04	3	8-Lead SOIC_N		-40 to +125	1,000
ADR445ARZ <sup>1</sup>	5.000	6	0.12	10	8-Lead SOIC_N		-40 to +125	98
ADR445ARZ-REEL7 <sup>1</sup>	5.000	6	0.12	10	8-Lead SOIC_N		-40 to +125	1,000
ADR445ARMZ <sup>1</sup>	5.000	6	0.12	10	8-Lead MSOP	R05	-40 to +125	98
ADR445ARMZ-REEL7 <sup>1</sup>	5.000	6	0.12	10	8-Lead MSOP	R05	-40 to +125	1,000
ADR445BRZ <sup>1</sup>	5.000	2	0.04	3	8-Lead SOIC_N		-40 to +125	98
ADR445BRZ-REEL7 <sup>1</sup>	5.000	2	0.04	3	8-Lead SOIC_N		-40 to +125	1,000

<sup>1</sup> Z = Pb-free part.

**NOTES**

Purchase of licensed I<sup>2</sup>C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system, provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips.