

# DATA SHEET

## **74HC154; 74HCT154** 4-to-16 line decoder/demultiplexer

Product specification  
Supersedes data of 2004 Oct 05

2004 Oct 12

## 4-to-16 line decoder/demultiplexer

## 74HC154; 74HCT154

## FEATURES

- 16-line demultiplexing capability
- Decodes 4 binary-coded inputs into one 16 mutually exclusive outputs
- Complies with JEDEC standard no. 8-1 B
- ESD protection:  
HBM EIA/JESD22-A114-B exceeds 2000 V  
MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ .

## DESCRIPTION

The 74HC154; 74HCT154 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC154; 74HCT154 decoders accept four active HIGH binary address inputs and provide 16 mutually exclusive active LOW outputs. The two-input enable gate can be used to strobe the decoder to eliminate the normal decoding "glitches" on the outputs, or can be used for the expansion of the decoder.

The enable gate has two ANDed inputs which must be LOW to enable the outputs.

The 74HC154; 74HCT154 can be used as a 1-to-16 demultiplexer by using one of the enable inputs as the multiplexed data input.

When the other enable input is LOW, the addressed output will follow the state of the applied data.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 6\text{ ns}$ .

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			74HC154	74HCT154	
$t_{\text{PHL}}/t_{\text{PLH}}$	propagation delay $A_n, \overline{E}_n$ to $\overline{Y}_n$	$C_L = 15\text{ pF}$ ; $R_L = 1\text{ k}\Omega$ ; $V_{\text{CC}} = 5\text{ V}$	11	13	ns
$C_I$	input capacitance		3.5	3.5	pF
$C_{\text{PD}}$	power dissipation capacitance per gate	notes 1 and 2	60	60	pF

## Notes

1.  $C_{\text{PD}}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{\text{PD}} \times V_{\text{CC}}^2 \times f_i \times N + \Sigma(C_L \times V_{\text{CC}}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{\text{CC}}$  = supply voltage in Volts;

$N$  = total load switching outputs;

$\Sigma(C_L \times V_{\text{CC}}^2 \times f_o)$  = sum of the outputs.

2. For 74HC154 the condition is  $V_I = \text{GND to } V_{\text{CC}}$   
For 74HCT154 the condition is  $V_I = \text{GND to } V_{\text{CC}} - 1.5\text{ V}$ .

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**FUNCTION TABLE**

See note 1.

INPUT						OUTPUT																		
E0	E1	A0	A1	A2	A3	Y0	Y1	Y2	Y3	Y4	Y6	Y7	Y8	Y2	Y9	Y10	Y11	Y12	Y13	Y14	Y15			
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H		
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H		
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H		
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H		
		H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	
		L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	
		H	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	
		L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	
		H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
		L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
		H	H	H	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
		L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
		H	L	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
		L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
		H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
		L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
		H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
		L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
		H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

**Note**

- 1. H = HIGH voltage level
- L = LOW voltage level
- X = don't care.

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## ORDERING INFORMATION

TYPE NUMBER	TEMPERATURE RANGE	PACKAGE			
		PINS	PACKAGE	MATERIAL	CODE
74HC154N	-40 °C to +125 °C	24	DIP24	plastic	SOT101-1
74HCT154N	-40 °C to +125 °C	24	DIP24	plastic	SOT101-1
74HC154D	-40 °C to +125 °C	24	SO24	plastic	SOT137-1
74HCT154D	-40 °C to +125 °C	24	SO24	plastic	SOT137-1
74HC154DB	-40 °C to +125 °C	24	SSOP24	plastic	SOT340-1
74HCT154DB	-40 °C to +125 °C	24	SSOP24	plastic	SOT340-1
74HC154PW	-40 °C to +125 °C	24	TSSOP24	plastic	SOT355-1
74HCT154PW	-40 °C to +125 °C	24	TSSOP24	plastic	SOT355-1
74HC154BQ	-40 °C to +125 °C	24	DHVQFN24	plastic	SOT815-1
74HCT154BQ	-40 °C to +125 °C	24	DHVQFN24	plastic	SOT815-1

## PINNING

PIN	SYMBOL	DESCRIPTION
1	$\overline{Y0}$	data output (active LOW)
2	$\overline{Y1}$	data output (active LOW)
3	$\overline{Y2}$	data output (active LOW)
4	$\overline{Y3}$	data output (active LOW)
5	$\overline{Y4}$	data output (active LOW)
6	$\overline{Y5}$	data output (active LOW)
7	$\overline{Y6}$	data output (active LOW)
8	$\overline{Y7}$	data output (active LOW)
9	$\overline{Y8}$	data output (active LOW)
10	$\overline{Y9}$	data output (active LOW)
11	$\overline{Y10}$	data output (active LOW)
12	GND	ground (0 V)
13	$\overline{Y11}$	data output (active LOW)
14	$\overline{Y12}$	data output (active LOW)
15	$\overline{Y13}$	data output (active LOW)
16	$\overline{Y14}$	data output (active LOW)
17	$\overline{Y15}$	data output (active LOW)
18	$\overline{E0}$	enable input
19	$\overline{E1}$	enable input
20	A3	data input
21	A2	data input
22	A1	data input
23	A0	data input
24	V <sub>CC</sub>	positive supply voltage

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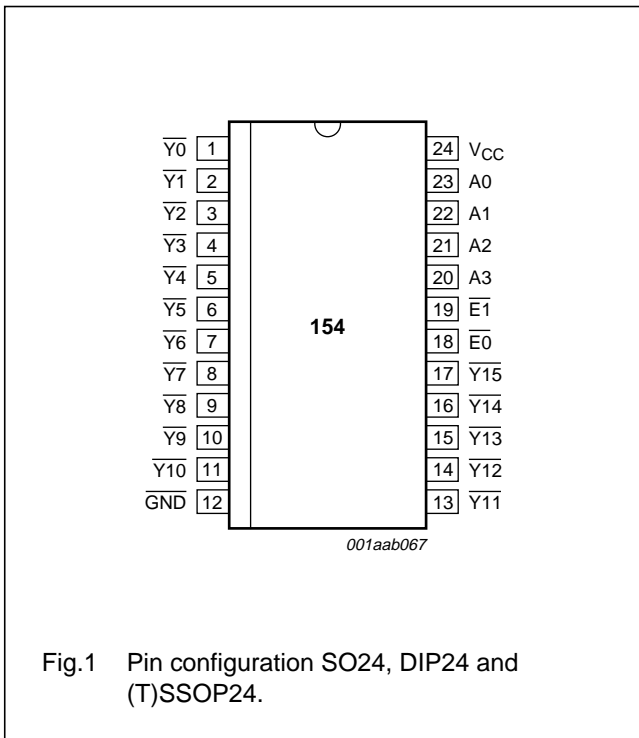
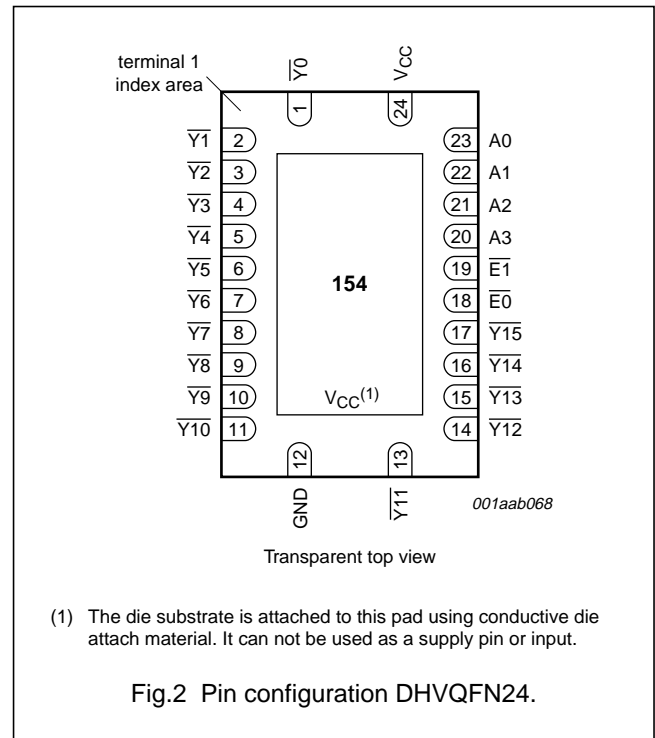


Fig.1 Pin configuration SO24, DIP24 and (T)SSOP24.



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN24.

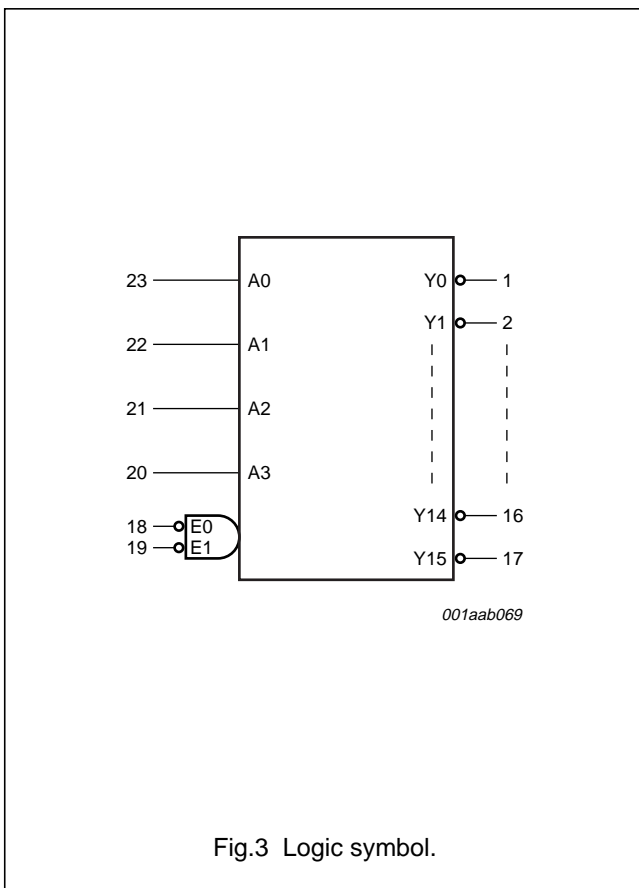


Fig.3 Logic symbol.

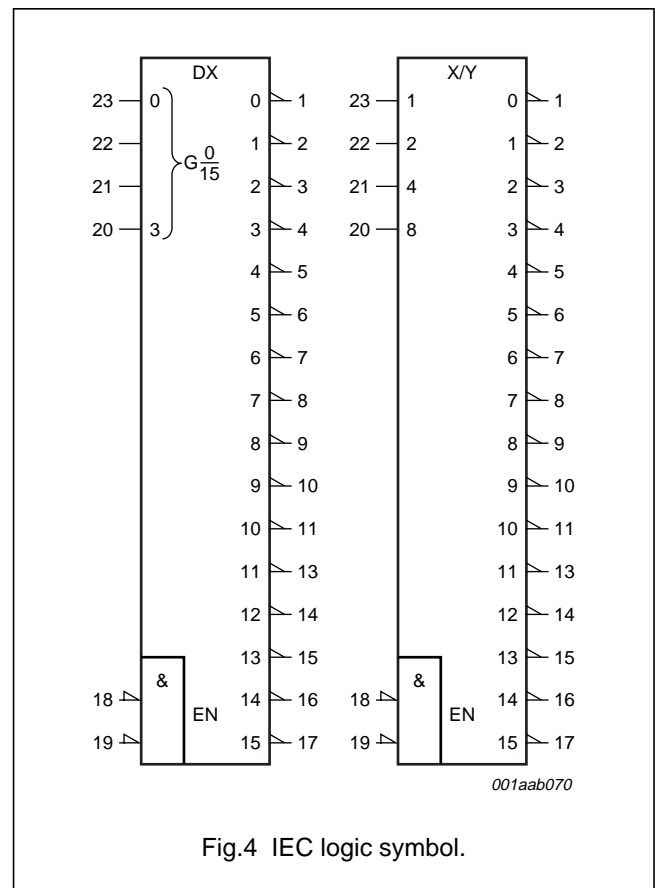
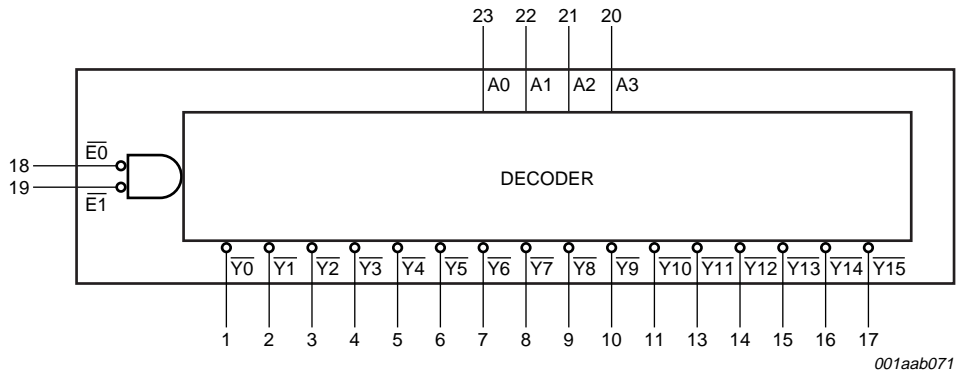


Fig.4 IEC logic symbol.

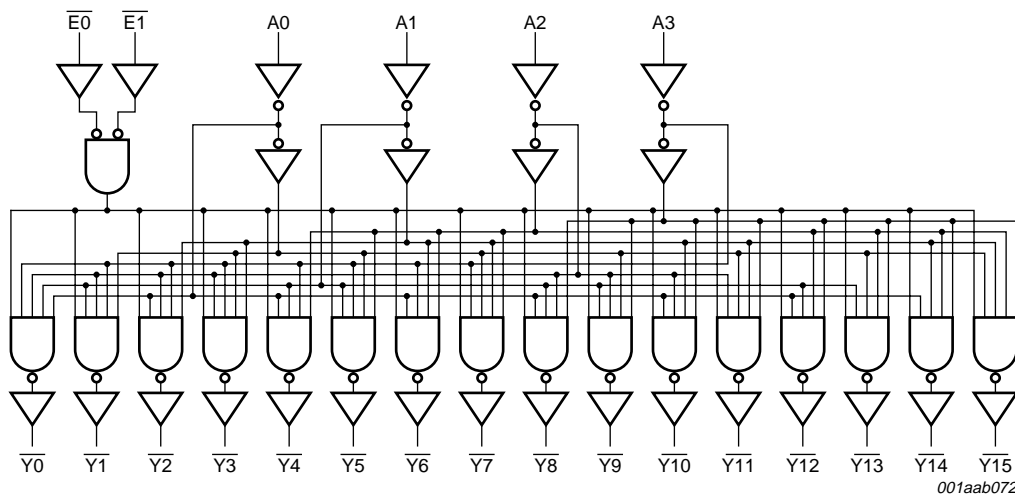
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001aab071

Fig.5 Functional diagram.



001aab072

Fig.6 Logic diagram.

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC154			74HCT154			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
$V_{CC}$	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
$V_I$	input voltage		0	–	$V_{CC}$	0	–	$V_{CC}$	V
$V_O$	output voltage		0	–	$V_{CC}$	0	–	$V_{CC}$	V
$T_{amb}$	ambient temperature		–40	+25	+125	–40	+25	+125	°C
$t_r, t_f$	input rise and fall times	$V_{CC} = 2.0\text{ V}$	–	–	1000	–	–	–	ns
		$V_{CC} = 4.5\text{ V}$	–	6.0	500	–	6.0	500	ns
		$V_{CC} = 6.0\text{ V}$	–	–	400	–	–	–	ns

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		–0.5	+7.0	V
$I_{IK}$	input diode current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ ; note 1	–	±20	mA
$I_{OK}$	output diode current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ ; note 1	–	±20	mA
$I_O$	output source or sink current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$ ; note 1	–	±25	mA
$I_{CC}, I_{GND}$	$V_{CC}$ or GND current	note 1	–	±50	mA
$T_{stg}$	storage temperature		–65	+150	°C
$P_{tot}$	power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ ; note 2	–	300	mW

## Notes

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- For DIP24 packages: above 70 °C the value of  $P_{tot}$  derates linearly with 12 mW/K.  
For SO24 packages: above 70 °C the value of  $P_{tot}$  derates linearly with 8 mW/K.  
For SSOP24 and TSSOP24 packages: above 60 °C the value of  $P_{tot}$  derates linearly with 5.5 mW/K.  
For DHVQFN24 packages: above 60 °C the value of  $P_{tot}$  derates linearly with 4.5 mW/K.

## 4-to-16 line decoder/demultiplexer

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## DC CHARACTERISTICS

## Type 74HC154

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = 25 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		2.0	1.5	1.2	–	V
			4.5	3.15	2.4	–	V
			6.0	4.2	3.2	–	V
V <sub>IL</sub>	LOW-level input voltage		2.0	–	0.8	0.5	V
			4.5	–	2.1	1.35	V
			6.0	–	2.8	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = –20 µA	2.0	1.9	2.0	–	V
		I <sub>O</sub> = –20 µA	4.5	4.4	4.5	–	V
		I <sub>O</sub> = –20 µA	6.0	5.9	6.0	–	V
		I <sub>O</sub> = –4.0 mA	4.5	3.98	4.32	–	V
		I <sub>O</sub> = –5.2 mA	6.0	5.48	5.81	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20 µA	2.0	–	0	0.1	V
		I <sub>O</sub> = 20 µA	4.5	–	0	0.1	V
		I <sub>O</sub> = 20 µA	6.0	–	0	0.1	V
		I <sub>O</sub> = 4.0 mA	4.5	–	0.15	0.26	V
		I <sub>O</sub> = 5.2 mA	6.0	–	0.16	0.26	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	6.0	–	–	±0.1	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	6.0	–	–	8.0	µA



4-to-16 line decoder/demultiplexer

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SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		2.0	1.5	-	-	V
			4.5	3.15	-	-	V
			6.0	4.2	-	-	V
V <sub>IL</sub>	LOW-level input voltage		2.0	-	-	0.5	V
			4.5	-	-	1.35	V
			6.0	-	-	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -20 μA	2.0	1.9	-	-	V
		I <sub>O</sub> = -20 μA	4.5	4.4	-	-	V
		I <sub>O</sub> = -20 μA	6.0	5.9	-	-	V
		I <sub>O</sub> = -4.0 mA	4.5	3.84	-	-	V
		I <sub>O</sub> = -5.2 mA	6.0	5.34	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20 μA	2.0	-	-	0.1	V
		I <sub>O</sub> = 20 μA	4.5	-	-	0.1	V
		I <sub>O</sub> = 20 μA	6.0	-	-	0.1	V
		I <sub>O</sub> = 4.0 mA	4.5	-	-	0.33	V
		I <sub>O</sub> = 5.2 mA	6.0	-	-	0.33	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	6.0	-	-	±1.0	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	6.0	-	-	80	μA

## 4-to-16 line decoder/demultiplexer

## 74HC154; 74HCT154

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		2.0	1.5	–	–	V
			4.5	3.15	–	–	V
			6.0	4.2	–	–	V
V <sub>IL</sub>	LOW-level input voltage		2.0	–	–	0.5	V
			4.5	–	–	1.35	V
			6.0	–	–	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -20 μA	2.0	1.9	–	–	V
		I <sub>O</sub> = -20 μA	4.5	4.4	–	–	V
		I <sub>O</sub> = -20 μA	6.0	5.9	–	–	V
		I <sub>O</sub> = -4.0 mA	4.5	3.7	–	–	V
		I <sub>O</sub> = -5.2 mA	6.0	5.2	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20 μA	2.0	–	–	0.1	V
		I <sub>O</sub> = 20 μA	4.5	–	–	0.1	V
		I <sub>O</sub> = 20 μA	6.0	–	–	0.1	V
		I <sub>O</sub> = 4.0 mA	4.5	–	–	0.4	V
		I <sub>O</sub> = 5.2 mA	6.0	–	–	0.4	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	6.0	–	–	±0.1	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	6.0	–	–	160	μA

## 4-to-16 line decoder/demultiplexer

## 74HC154; 74HCT154

**Type 74HCT154**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = 25 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		4.5 to 5.5	2.0	1.6	–	V
V <sub>IL</sub>	LOW-level input voltage		4.5 to 5.5	–	1.2	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = –20 µA	4.5	4.4	4.5	–	V
		I <sub>O</sub> = –4 mA	4.5	3.98	4.32	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20 µA	4.5	–	0	0.1	V
		I <sub>O</sub> = 4 mA	4.5	–	0.15	0.25	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	–	–	±0.1	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	5.5	–	–	8.0	µA
ΔI <sub>CC</sub>	additional quiescent supply current per input	V <sub>I</sub> = V <sub>CC</sub> – 2.1 V; I <sub>O</sub> = 0 A	4.5 to 5.5	–	–	360	µA
<b>T<sub>amb</sub> = –40 °C to +85 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = –20 µA	4.5	4.4	–	–	V
		I <sub>O</sub> = –4 mA	4.5	3.84	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20 µA	4.5	–	–	0.1	V
		I <sub>O</sub> = 4 mA	4.5	–	–	0.33	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	–	–	±1.0	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	5.5	–	–	80	µA
ΔI <sub>CC</sub>	additional quiescent supply current per input	V <sub>I</sub> = V <sub>CC</sub> – 2.1 V; I <sub>O</sub> = 0 A	4.5 to 5.5	–	–	450	µA

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## 74HC154; 74HCT154

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -20 μA	4.5	4.4	–	–	V
		I <sub>O</sub> = -4 mA	4.5	3.7	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20 μA	4.5	–	–	0.1	V
		I <sub>O</sub> = 4 mA	4.5	–	–	0.4	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	–	–	±1.0	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	5.5	–	–	160	μA
ΔI <sub>CC</sub>	additional quiescent supply current per input	V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; I <sub>O</sub> = 0 A	4.5 to 5.5	–	–	490	μA

## 4-to-16 line decoder/demultiplexer

## 74HC154; 74HCT154

## AC CHARACTERISTICS

## Type 74HC154

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	$V_{CC}$ (V)				
<b><math>T_{amb} = 25</math> °C</b>							
$t_{PHL}/t_{PLH}$	propagation delay $A_n$ to $\overline{Y}_n$	see Figs 7 and 9	2.0	–	36	150	ns
			4.5	–	13	30	ns
			6.0	–	10	26	ns
	propagation delay $\overline{E}_n$ to $\overline{Y}_n$	see Figs 8 and 9	2.0	–	39	150	ns
			4.5	–	14	30	ns
			6.0	–	11	26	ns
$t_{THL}/t_{TLH}$	output transition time	see Figs 7, 8 and 9	2.0	–	19	75	ns
			4.5	–	7	15	ns
			6.0	–	6	13	ns
<b><math>T_{amb} = -40</math> °C to <math>+85</math> °C</b>							
$t_{PHL}/t_{PLH}$	propagation delay $A_n$ to $\overline{Y}_n$	see Figs 7 and 9	2.0	–	–	190	ns
			4.5	–	–	38	ns
			6.0	–	–	33	ns
	propagation delay $\overline{E}_n$ to $\overline{Y}_n$	see Figs 8 and 9	2.0	–	–	190	ns
			4.5	–	–	38	ns
			6.0	–	–	33	ns
$t_{THL}/t_{TLH}$	output transition time	see Figs 7, 8 and 9	2.0	–	–	95	ns
			4.5	–	–	19	ns
			6.0	–	–	16	ns
<b><math>T_{amb} = -40</math> °C to <math>+125</math> °C</b>							
$t_{PHL}/t_{PLH}$	propagation delay $A_n$ to $\overline{Y}_n$	see Figs 7 and 9	2.0	–	–	225	ns
			4.5	–	–	45	ns
			6.0	–	–	38	ns
	propagation delay $\overline{E}_n$ to $\overline{Y}_n$	see Figs 8 and 9	2.0	–	–	225	ns
			4.5	–	–	45	ns
			6.0	–	–	38	ns
$t_{THL}/t_{TLH}$	output transition time	see Figs 7, 8 and 9	2.0	–	–	110	ns
			4.5	–	–	22	ns
			6.0	–	–	19	ns

4-to-16 line decoder/demultiplexer

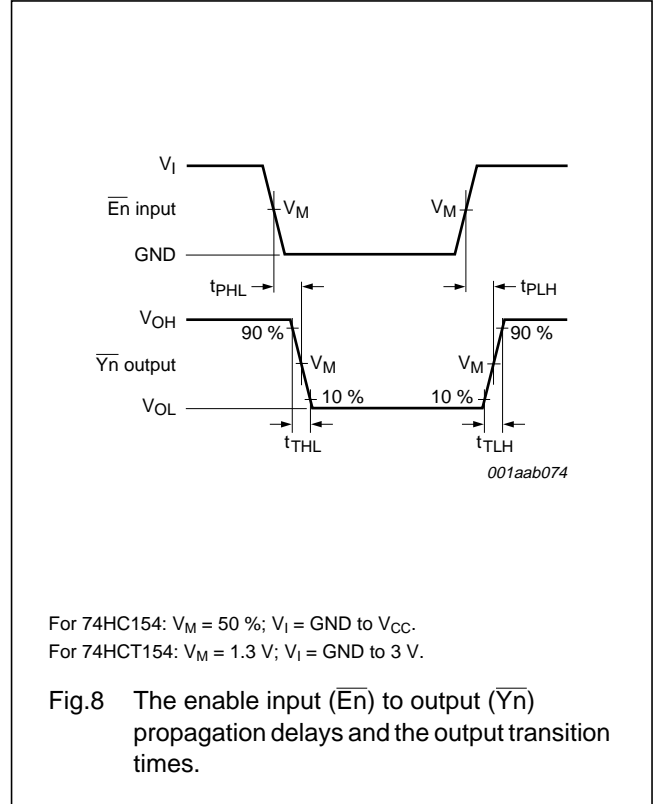
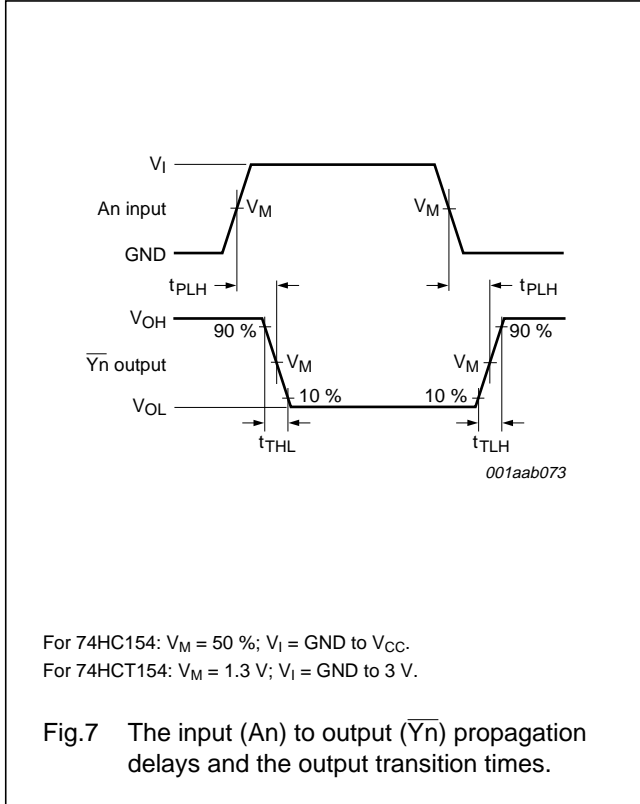
74HC154; 74HCT154

Type 74HCT154

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF.

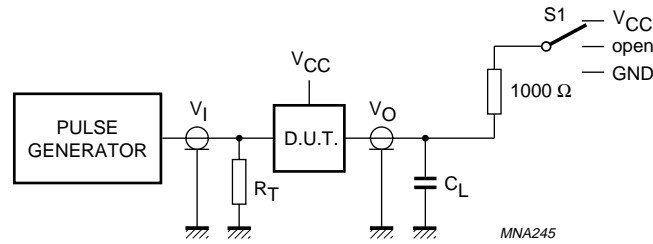
SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = 25 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay An to $\bar{Y}_n$	see Figs 7 and 9	4.5	–	16	35	ns
	propagation delay $\bar{E}_n$ to $\bar{Y}_n$	see Figs 8 and 9	4.5	–	15	32	ns
t <sub>THL</sub> /t <sub>TLH</sub>	output transition time	see Figs 7, 8 and 9	4.5	–	7	15	ns
<b>T<sub>amb</sub> = –40 °C to +85 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay An to $\bar{Y}_n$	see Figs 7 and 9	4.5	–	–	44	ns
	propagation delay $\bar{E}_n$ to $\bar{Y}_n$	see Figs 8 and 9	4.5	–	–	40	ns
t <sub>THL</sub> /t <sub>TLH</sub>	output transition time	see Figs 7, 8 and 9	4.5	–	–	19	ns
<b>T<sub>amb</sub> = –40 °C to +125 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay An to $\bar{Y}_n$	see Figs 7 and 9	4.5	–	–	53	ns
	propagation delay $\bar{E}_n$ to $\bar{Y}_n$	see Figs 8 and 9	4.5	–	–	48	ns
t <sub>THL</sub> /t <sub>TLH</sub>	output transition time	see Figs 7, 8 and 9	4.5	–	–	22	ns

AC WAVEFORMS



4-to-16 line decoder/demultiplexer

74HC154; 74HCT154



TEST	S1
$t_{PLH}/t_{PHL}$	open
$t_{PLZ}/t_{PZL}$	V <sub>CC</sub>
$t_{PHZ}/t_{PZH}$	GND

Definitions for test circuit:  
 C<sub>L</sub> = Load capacitance including jig and probe capacitance.  
 R<sub>T</sub> = Termination resistance should be equal to the output impedance Z<sub>o</sub> of the pulse generator.

Fig.9 Load circuitry for switching times.

APPLICATION DATA

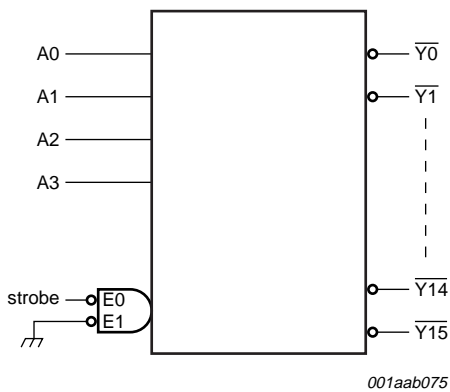


Fig.10 1-of-16 decoder; LOW level output selected.

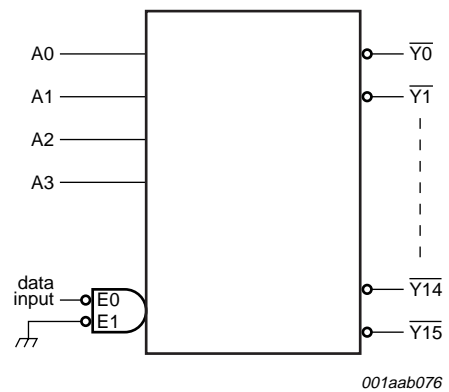


Fig.11 1-of-16 demultiplexer; logic level on selected outputs follow the logic level on the data input.

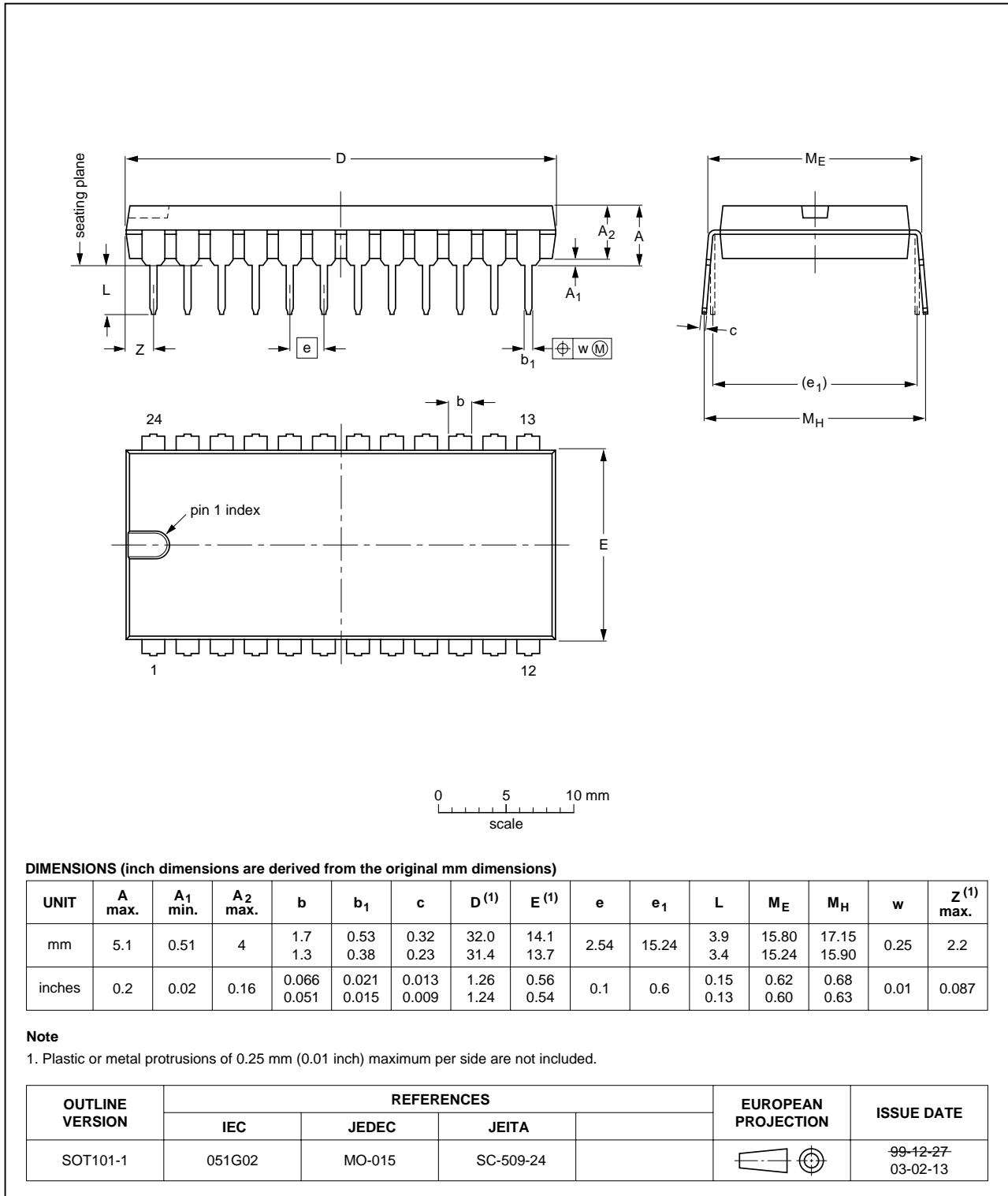
4-to-16 line decoder/demultiplexer

74HC154; 74HCT154

PACKAGE OUTLINES

DIP24: plastic dual in-line package; 24 leads (600 mil)

SOT101-1



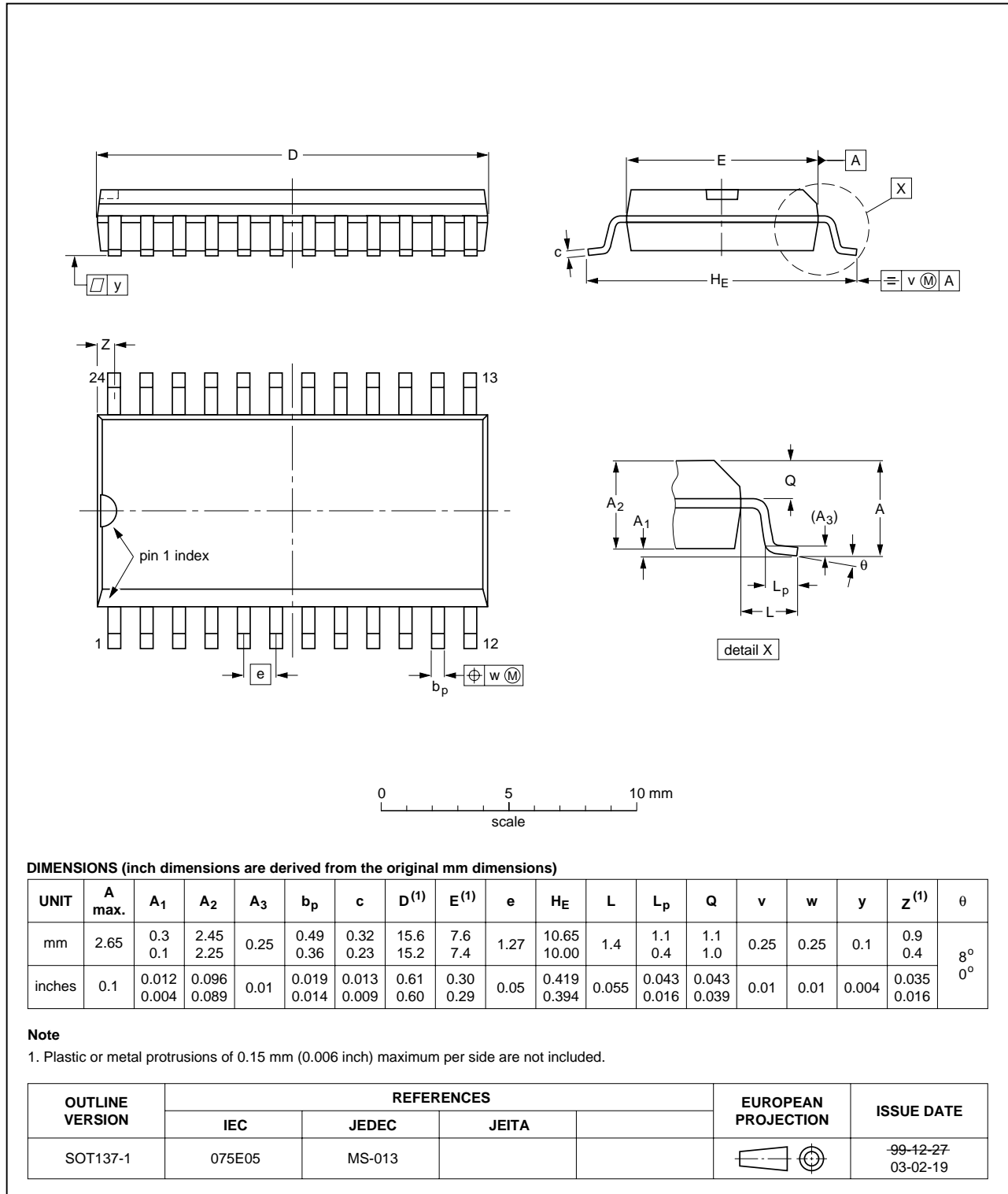


4-to-16 line decoder/demultiplexer

74HC154; 74HCT154

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

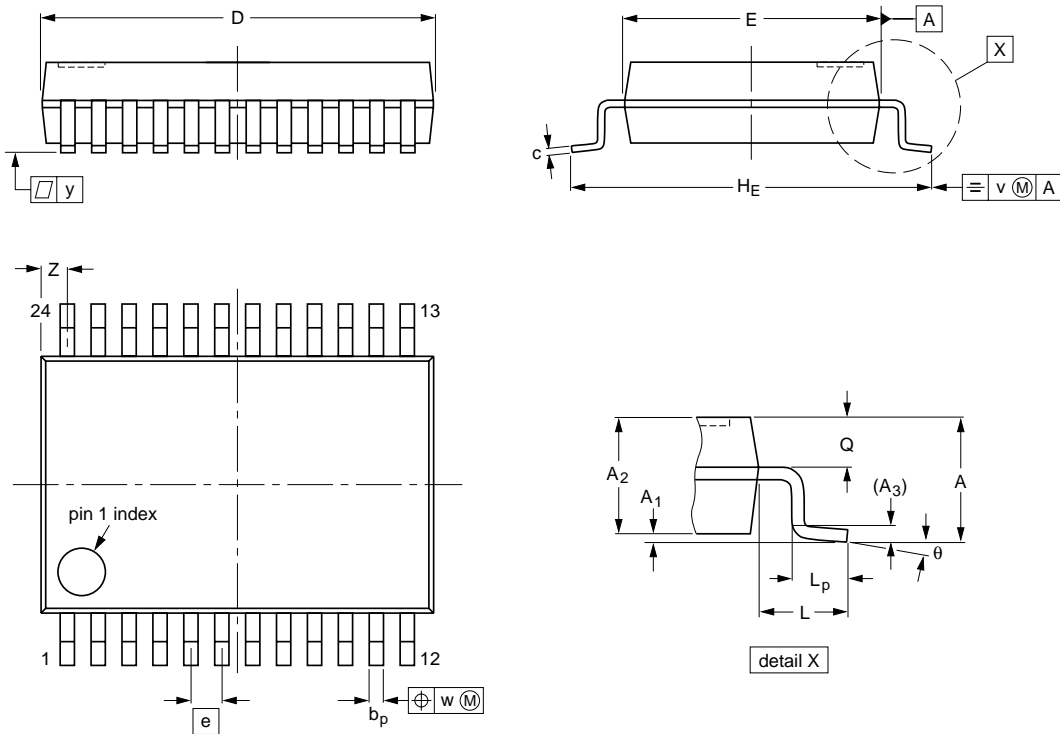


4-to-16 line decoder/demultiplexer

74HC154; 74HCT154

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

**Note**

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

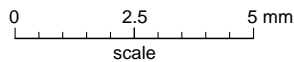
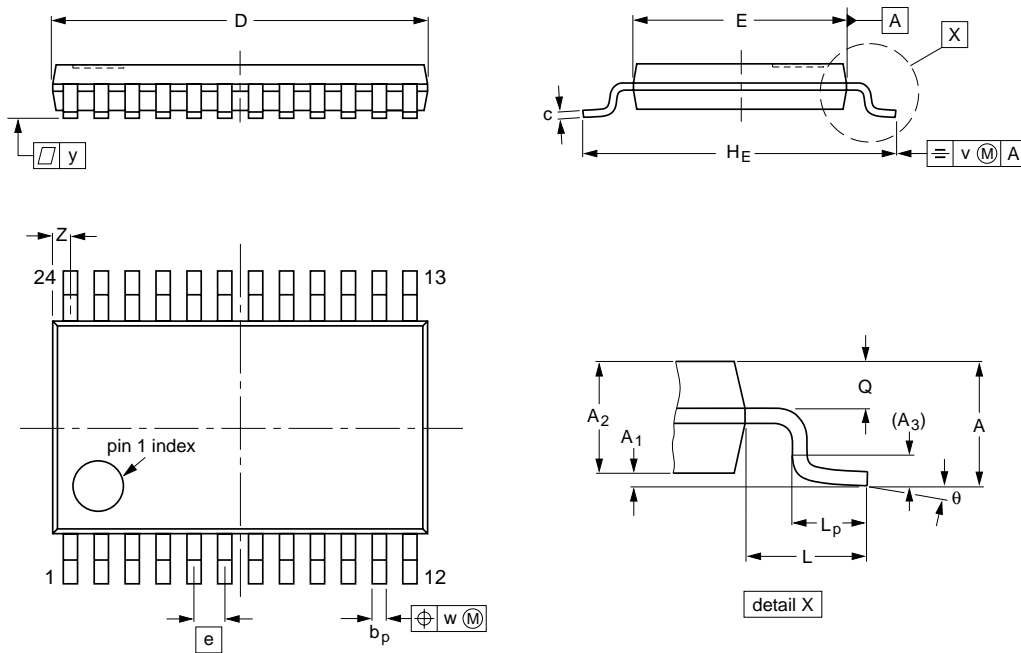
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				99-12-27 03-02-19

4-to-16 line decoder/demultiplexer

74HC154; 74HCT154

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

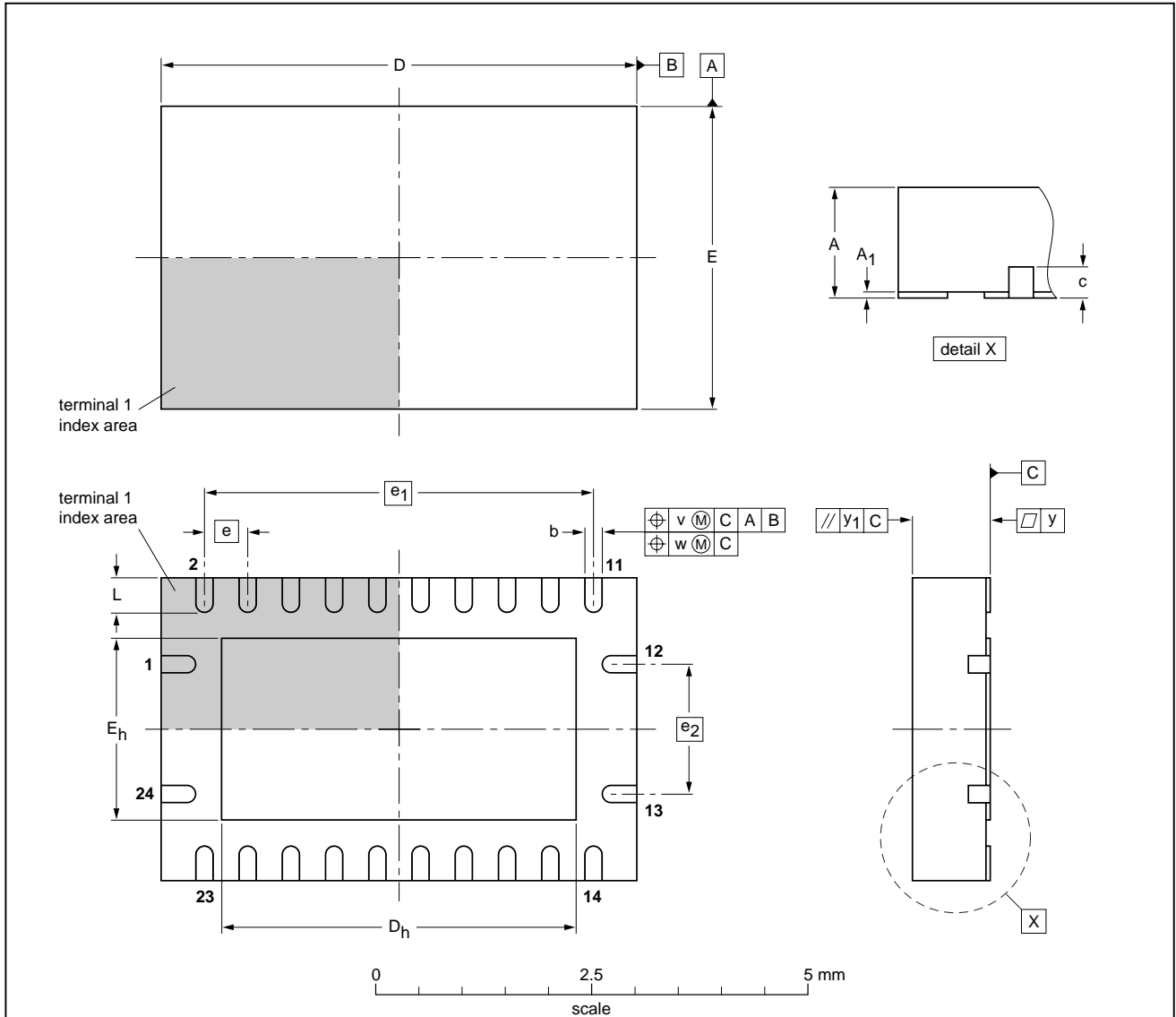
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				99-12-27 03-02-19

4-to-16 line decoder/demultiplexer

74HC154; 74HCT154

DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package;  
no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm

SOT815-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A <sup>(1)</sup> max.	A <sub>1</sub>	b	c	D <sup>(1)</sup>	D <sub>h</sub>	E <sup>(1)</sup>	E <sub>h</sub>	e	e <sub>1</sub>	e <sub>2</sub>	L	v	w	y	y <sub>1</sub>
mm	1	0.05 0.00	0.30 0.18	0.2	5.6 5.4	4.25 3.95	3.6 3.4	2.25 1.95	0.5	4.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT815-1	---	---	---			03-04-29

## 4-to-16 line decoder/demultiplexer

## 74HC154; 74HCT154

## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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