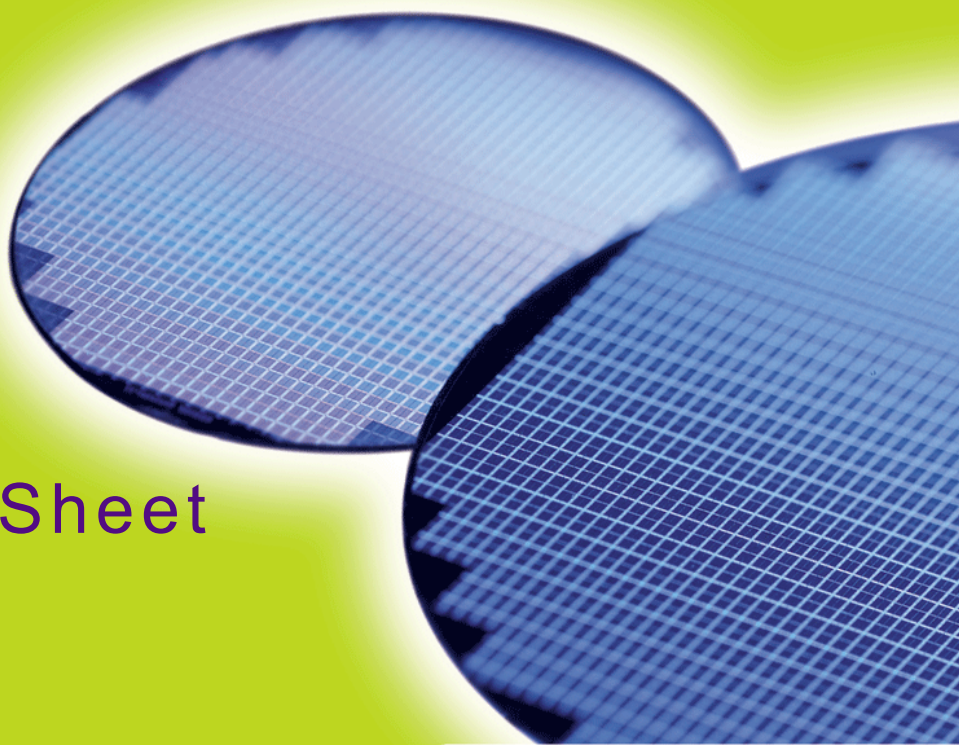


**HY[B/E]25L256160AC**  
**HY[B/E]25L256160AF**

*DRAMs for Mobile Applications*

*256-MBit Mobile-RAM*  
*RoHS compliant*



**Internet Data Sheet**

*Rev. 1.41*



HY[B/E]25L256160AC, HY[B/E]25L256160AF

**Revision History: 2006-12, Rev. 1.41**

Page	Subjects (major changes since last revision)
All	Adapted internet edition
All	New Qimonda Template

**Previous Revision: 2005-06, Rev. 1.4**

All	Added new Product Type
9	VDD: editorial change
2	Added disclaimer

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# 1 Overview

## 1.1 Features

- 16 Mbits × 16 organisation
- Fully synchronous to positive clock edge
- Four internal banks for concurrent operation
- Data mask (DM) for byte control with write and read data
- Programmable CAS latency: 2 or 3
- Programmable burst length: 1, 2, 4, 8, or full page
- Programmable wrap sequence: sequential or interleaved
- Random column address every clock cycle (1-N rule)
- Deep power down mode
- Extended mode register for Mobile-RAM features
- Temperature compensated self refresh with on-die temperature sensor
- Partial array self refresh
- Power down and clock suspend mode
- Automatic and controlled precharge command
- Auto refresh mode (CBR)
- 8192 refresh cycles / 64 ms
- Self-refresh with programmable refresh period
- Programmable power reduction feature by partial array activation during self-refresh
- $V_{DDQ} = 1.8V$  or  $2.5 V$  or  $3.3 V$
- $V_{DD} = 2.5 V$  or  $3.3 V$
- P-TFBGA-54 package 9-by-6-ball array with 3 depopulated rows ( $12 \times 8 \text{ mm}^2$ )
- Operating temperature range:  
commercial ( $0 \text{ }^\circ\text{C}$  to  $+70 \text{ }^\circ\text{C}$ )  
extended ( $-25 \text{ }^\circ\text{C}$  to  $+85 \text{ }^\circ\text{C}$ )

**Table 1 Performance** <sup>1)</sup>

Part Number Speed Code			-7.5	Unit
max. Clock Frequency	@CL3	$f_{CK3}$	133	MHz
min. Clock Period	@CL3	$t_{CK3}$	7.5	ns
min. Access Time from Clock	@CL3	$t_{AC3}$	6.0	ns
min. Clock Period	@CL2	$t_{CK2}$	9.5	ns
min. Access Time from Clock	@CL2	$t_{AC2}$	6.0	ns

1) for  $V_{DDQ} = 2.5 V$  or  $3.3 V$ ; see [Table 9](#) for  $V_{DDQ}$  dependent performance



## 1.2 Description

The 256MBit Mobile-RAM is a new generation of low power, four bank synchronous DRAM organized as 4 banks x 4 Mbit x 16 with additional features for mobile applications. The synchronous Mobile-RAM achieves high speed data transfer rates by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock.

The device adds new features to the industry standards set for synchronous DRAM products. Parts of the memory array can be selected for Self-Refresh and the refresh period during Self-Refresh is programmable in 4 steps which drastically reduces the self refresh current, depending on the case temperature of the components in the system application. In addition a “Deep Power Down Mode” is available. Operating the four memory banks in an interleave fashion allows random access operation to occur at higher rate. A sequential and gapless data rate is possible depending on burst length, CAS latency and speed grade of the device.

The Mobile-RAM is housed in a FBGA “chip-size” package. The Mobile-RAM is available in the commercial ( $0\text{ }^{\circ}\text{C} \leq \text{TC} \leq 70\text{ }^{\circ}\text{C}$ ) and extended ( $-25\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ) temperature range.

**Table 2 Ordering Information for Non-Green Products**

Product Type <sup>1)</sup>	Function Code	Case Temperature Range	Package
HYB25L256160AC-7.5	PC133-333-522	commercial ( $0\text{ }^{\circ}\text{C} \leq \text{TC} \leq 70\text{ }^{\circ}\text{C}$ )	P-TFBGA-54
HYE25L256160AC-7.5	PC133-333-522	extended ( $-25\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ )	P-TFBGA-54

**Table 3 Ordering Information for Green Products**



Product Type <sup>1)</sup>	Function Code	Case Temperature Range	Package
HYB25L256160AF-7.5	PC133-333-522	commercial ( $0\text{ }^{\circ}\text{C} \leq \text{TC} \leq 70\text{ }^{\circ}\text{C}$ )	P-TFBGA-54
HYE25L256160AF-7.5	PC133-333-522	extended ( $-25\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ )	P-TFBGA-54

- 1) HYB/E: designator for memory components for commercial /extended temperature range  
 25L: Mobile-RAM at  $V_{DD} = 2.5\text{ V}$   
 256: 256-Mbit density  
 160: Product variation x16  
 A: Die revision A  
 F/C: Lead & Halogen free / Lead-Containing  
 -7.5: speed grade - see [Table 1](#)



## 2 Pin Configuration

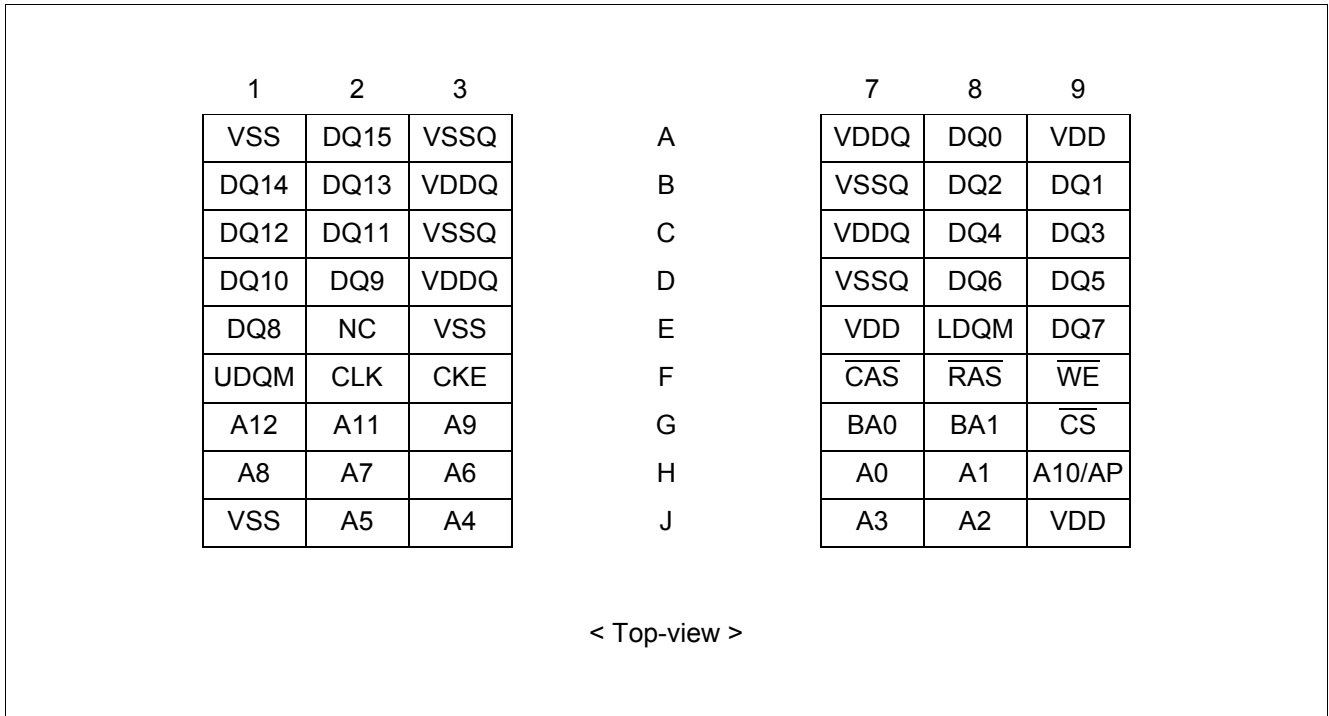


Figure 1 Pin Configuration P-TFBGA-54 (16 Mb × 16)



**Table 4 Input/Output Signals**

Pin	Symbol	Type	Polarity	Function			
F2	CLK	Input	Positive Edge	<b>Clock</b>			
F3	CKE	Input	Active High	<b>Clock Enable</b>			
G9	$\overline{\text{CS}}$	Input	Active Low	<b>Chip Select</b>			
F8	$\overline{\text{RAS}}$	Input	Active Low	<b>Command Inputs</b>			
F7	$\overline{\text{CAS}}$						
F9	$\overline{\text{WE}}$						
G8	BA1	Input	Active High	<b>Bank Address Inputs</b>			
G7	BA0						
G1	A12	Input	Active High	<b>Address Inputs</b>			
G2	A11						
H9	A10/AP						
G3	A9						
H1	A8						
H2	A7						
H3	A6						
J2	A5						
J3	A4						
J7	A3						
J8	A2						
H8	A1						
H7	A0						
A2	DQ15				Input/Output	Active High	<b>Data Input/Output</b>
B1	DQ14						
B2	DQ13						
C1	DQ12						
C2	DQ11						
D1	DQ10						
D2	DQ9						
E1	DQ8						
E9	DQ7						
D8	DQ6						
D9	DQ5						
C8	DQ4						
C9	DQ3						
B8	DQ2						
B9	DQ1						
A8	DQ0						



Table 4 Input/Output Signals (cont'd)

Pin	Symbol	Type	Polarity	Function
F1	UDQM	Input	Active High	Data Input/Output Mask
E8	LDQM			
E2	NC	—	—	Not Connected
A7 B3 C7 D3	$V_{DDQ}$	Supply	—	DQ Power Supply
A3 B7 C3 D7	$V_{SSQ}$	Supply	—	DQ Ground
A9 E7 J9	$V_{DD}$	Supply	—	Power Supply
A1 E3 J1	$V_{SS}$	Supply	—	Ground



### 3 Functional Description

#### MR

#### Mode Register Definition

(BA[1:0] = 00<sub>B</sub>)

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	MODE						CL		BT	BL			
reg. addr		w						w		w	w			

Field	Bits	Type	Description
BL	[2:0]	w	<b>Burst Length</b> Number of sequential bits per DQ related to one read/write command. <i>Note: All other bit combinations are RESERVED.</i>  000 1 001 2 010 4 011 8 111 full page (sequential burst type only)
BT	3	w	<b>Burst Type</b> See <a href="#">Table 5</a> for internal address sequence of low order address bits. 0 Sequential 1 Interleaved
CL	[6:4]	w	<b>CAS Latency</b> <i>Note: All other bit combinations are RESERVED.</i>  010 2 011 3
MODE	[12:7]	w	<b>Operating Mode</b> <i>Note: All other bit combinations are RESERVED.</i>  000000 Burst Read/Burst Write 000100 Burst Read/Single Write





**Table 5 Burst Definition**

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
	A2	A1	A0	Type = Sequential	Type = Interleaved
2			0	0-1	0-1
			1	1-0	1-0
4		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

**Notes:**

1. For a burst length of two, Ai-A1 selects the two-data-element block; A0 selects the first access within the block.
2. For a burst length of four, Ai-A2 selects the four-data-element block; A1-A0 selects the first access within the block.
3. For a burst length of eight, Ai-A3 selects the eight-data- element block; A2-A0 selects the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.



**EMR**

**Extended Mode Register Definition (BA[1:0] = 10<sub>B</sub>)**

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	MODE						TCSR			PASR			
reg. addr		w						w			w			

Field	Bits	Type	Description <sup>1)</sup>
<b>PASR</b>	[2:0]	w	<b>Partial Array Self Refresh</b> 000 banks to be self refreshed: all 4 of 4 001 banks to be self refreshed: 2 of 4, BA[1:0] = 00 <sub>B</sub> or 01 <sub>B</sub> 010 banks to be self refreshed: 1 of 4, BA[1:0] = 00 <sub>B</sub> 101 banks to be self refreshed: 0.5 of 4, BA[1:0] = 00 <sub>B</sub> & RA12 = 0 <sub>B</sub> 110 banks to be self refreshed: 0.25 of 4, BA[1:0] = 00 <sub>B</sub> & RA[12:11] = 00 <sub>B</sub>
<b>TCSR</b>	[4:3]	w	<b>Temperature Compensated Self Refresh</b> 00 on-chip temperature sensor enabled 01 Maximum case temperature: 45°C, on-chip temperature sensor disabled 10 Maximum case temperature: 15°C, on-chip temperature sensor disabled 11 Maximum case temperature: 85°C, on-chip temperature sensor disabled
<b>MODE</b>	[12:5]	w	<b>Operating Mode</b> 00h Normal operation

1) All other bit combinations are RESERVED.



## 4 Electrical Characteristics

### 4.1 Operating Conditions

Table 6 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Voltage on I/O pins relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-1.0	—	$V_{DD} + 0.5$	V	
Voltage on I/O pins relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-1.0	—	+4.6	V	
Voltage on $V_{DD}$ supply relative to $V_{SS}$	$V_{DD}$	-1.0	—	+4.6	V	
Voltage on $V_{DDQ}$ supply relative to $V_{SS}$	$V_{DDQ}$	-1.0	—	+4.6	V	
Operating Case Temperature (extended)	$T_{CASE}$	-25	—	+85	°C	
Storage Temperature (Plastic)	$T_{STG}$	-55	—	+150	°C	
Power Dissipation	$P_D$	—	—	0.7	W	
Short Circuit Output Current	$I_{OUT}$	—	50	—	mA	

**Attention:** Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 7 Recommended Operating Conditions and DC Characteristics<sup>1)</sup>

Parameter	Symbol	Values		Unit	Note/ Test Condition
		min.	max.		
Supply Voltage	$V_{DD}$	+2.3	+3.6	V	
I/O Supply Voltage	$V_{DDQ}$	+1.65	+3.6	V	2)
Supply Voltage	$V_{SS}$	0	0	V	
I/O Supply Voltage	$V_{SSQ}$	0	0	V	
Input High (Logic 1) Voltage	$V_{IH}$	$0.8 \times V_{DDQ}$	$V_{DDQ} + 0.3$	V	3)4)
Input Low (Logic 0) Voltage	$V_{IL}$	-0.3	+0.3	V	3)4)
Output High (Logic 1) Voltage	$V_{OH}$	$V_{DDQ} - 0.2$	—	V	$I_{OH} = -0.1$ mA
Output Low (Logic 0) Voltage	$V_{OL}$	—	+0.2	V	$I_{OH} = +0.1$ mA
Input Leakage Current	$I_{IL}$	-5	+5	μA	Any input $0 \text{ V} \leq V_{IN} \leq V_{DD}$ ; all other pins not under test $V_{IN} = 0 \text{ V}$
Output Leakage Current	$I_{OZ}$	-5	+5	μA	DQ is disabled; $0 \text{ V} \leq V_{OUT} \leq V_{DDQ}$

1)  $0 \text{ °C} \leq T_C \leq 70 \text{ °C}$  (comm.) and  $-25 \text{ °C} \leq T_{CASE} \leq +85 \text{ °C}$

2)  $V_{DDQ} < V_{DD} + 0.3 \text{ V}$

3) All voltages referenced to  $V_{SS}$

4)  $V_{IH}$  may overshoot to  $V_{DDQ} + 2.0 \text{ V}$  for pulse width of  $< 4 \text{ ns}$ .

$V_{IL}$  may undershoot to  $-2.0 \text{ V}$  for pulse width  $< 4 \text{ ns}$ .

Pulse width measured at 50% points with amplitude measured peak to DC reference



**Table 8 Input and Output Capacitances**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Input Capacitance: CLK	$C_{I1}$	—	—	3.5	pF	1)
Input Capacitance: All other input-only pins	$C_{I2}$	—	—	3.8	pF	1)
Input/Output Capacitance: DQ	$C_{I0}$	4.0	—	5.0	pF	1)

1) These values are guaranteed by design and are tested on a sample base only.  $V_{DDQ} = V_{DD} = 2.5 \text{ V} \pm 0.2 \text{ V}$ ,  $f = 1 \text{ MHz}$ ,  $T_{CASE} = 25 \text{ }^\circ\text{C}$ ,  $V_{OUT(DC)} = V_{DDQ}/2$ ,  $V_{OUT}$  (Peak to Peak) 0.2 V. Unused pins are tied to ground.

## 4.2 Timing Characteristics

**Table 9 AC Timing Characteristics<sup>1)2)</sup>**

Parameter	Symbol	–7.5		Unit	Note/ Test Condition
		min.	max.		
<b>Clock</b>					
DQ output access time from CLK	$t_{AC3}$	—	7.5	ns	$V_{DDQ} < 2.3 \text{ V}$ <sup>3)4)5)8)</sup>
		—	6	ns	$V_{DDQ} \geq 2.3 \text{ V}$ <sup>3)4)5)8)</sup>
		—	5.4	ns	$V_{DDQ} \geq 3.0 \text{ V}$ <sup>3)4)5)8)</sup>
	$t_{AC2}$	—	7.5	ns	$V_{DDQ} < 2.3 \text{ V}$ <sup>3)4)5)8)</sup>
		—	6	ns	$V_{DDQ} \geq 2.3 \text{ V}$ <sup>3)4)5)8)</sup>
		—	—	—	—
CK high-level width	$t_{CH}$	2.5	—	ns	—
CK low-level width	$t_{CL}$	2.5	—	ns	—
Clock cycle time	$t_{CK3}$	7.5	—	ns	$V_{DDQ} \geq 2.3 \text{ V}$ <sup>3)</sup>
		8	—	ns	$V_{DDQ} < 2.3 \text{ V}$ <sup>3)</sup>
	$t_{CK2}$	9.5	—	ns	<sup>3)</sup>
Clock frequency	$f_{CK3}$	—	133	MHz	$V_{DDQ} \geq 2.3 \text{ V}$ <sup>3)</sup>
		—	125	MHz	$V_{DDQ} < 2.3 \text{ V}$ <sup>3)</sup>
	$f_{CK2}$	—	105	MHz	<sup>3)</sup>

### Setup and Hold Times

Input setup time	$t_{IS}$	1.5	—	ns	6)
Input hold time	$t_{IH}$	0.8	—	ns	6)
CKE setup time	$t_{CKS}$	1.5	—	ns	6)
CKE hold time	$t_{CKH}$	0.8	—	ns	6)
Mode register setup time	$t_{RSC}$	2	—	$t_{CK}$	
Power down moder entry time	$t_{SB}$	0	7.5	ns	

### Common Parameters

Active to Read or Write delay	$t_{RCD}$	19	—	ns	7)
Precharge command period	$t_{RP}$	19	—	ns	7)
Active to Precharge command	$t_{RAS}$	45	100000	ns	7)
Active bank A to Active bank A period	$t_{RC}$	67	—	ns	7)
Active bank A to Active bank B delay	$t_{RRD}$	15	—	ns	7)
CAS to CAS command delay	$t_{CCD}$	1	—	$t_{CK}$	



Table 9 AC Timing Characteristics<sup>1)2)</sup> (cont'd)

Parameter	Symbol	-7.5		Unit	Note/ Test Condition
		min.	max.		
<b>Refresh Cycle</b>					
Refresh period	$t_{REF}$	—	64	ms	
Self refresh exit time	$t_{SREX}$	1	—	$t_{CK}$	
<b>Read Cycle</b>					
Data output hold time	$t_{OH}$	3	—	ns	4)7)8)
Data output from high to low impedance	$t_{LZ}$	1	—	ns	
Data output from low to high impedance	$t_{HZ}$	3	7	ns	
DQM data output disable latency	$t_{DQZ}$	—	2	$t_{CK}$	
<b>Write Cycle</b>					
Write recovery time	$t_{WR}$	14	—	ns	9)
DQM write data mask latency	$t_{DQW}$	0	—	$t_{CK}$	

- 1)  $0\text{ }^{\circ}\text{C} \leq T_C \leq 70\text{ }^{\circ}\text{C}$  (comm.) and  $-25\text{ }^{\circ}\text{C} \leq T_{CASE} \leq +85\text{ }^{\circ}\text{C}$ ; recommended operating conditions unless otherwise noted
- 2) For proper power-up see the operation section of this data sheet.
- 3) Symbol index 2 and 3 refer to CL = 2 and CL = 3.
- 4) AC timing tests are referenced to the 0.9 V crossover point. The transition time is measured between  $V_{IH}$  and  $V_{IL}$ . All AC measurements assume  $t_T = 1\text{ ns}$  with the AC output load circuit (details will be defined later). Specified  $t_{AC}$  and  $t_{OH}$  parameters are measured with a 30 pF only, without any resistive termination and with a input signal of 1V/ns edge rate (see Figure 2).
- 5) If clock rising time is longer than 1 ns, a time  $(t_T/2 - 0.5)\text{ ns}$  has to be added to this parameter.
- 6) If  $t_T$  is longer than 1 ns, a time  $(t_T - 1)\text{ ns}$  has to be added to this parameter.
- 7) These parameter account for the number of clock cycle and depend on the operating frequency of the clock, as follows:  
*the number of clock cycle = specified value of timing period (counted in fractions as a whole number)*
- 8) Access time from clock  $t_{AC}$  is 4.6 ns for -7.5 components with no termination and 0 pF load, Data out hold time  $t_{OH}$  is 1.8 ns for -7.5 components with no termination and 0 pF load.
- 9) The write recovery time of  $t_{WR} = 14\text{ ns}$  allows the use of one clock cycle for the write recovery time when the memory operation frequency is equal or less than 72MHz. For all memory operation frequencies higher than 72MHz two clock cycles for  $t_{WR}$  are mandatory. QIMONDA recommends to use two clock cycles for the write recovery time in all applications.

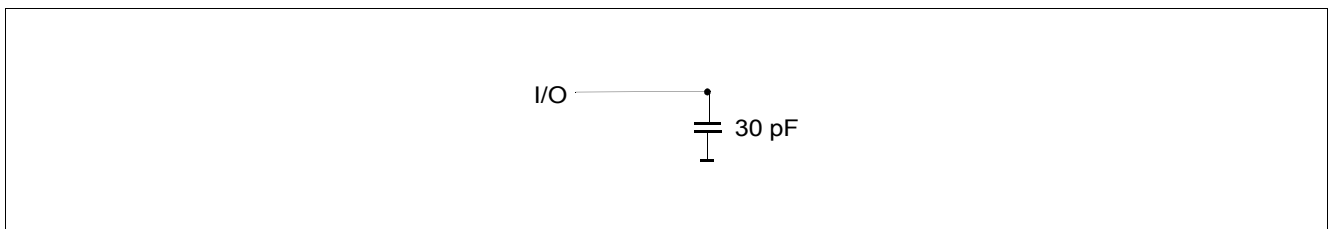


Figure 2 Measurement Conditions for  $t_{AC}$  and  $t_{OH}$



### 4.3 Current Specification

Table 10  $I_{DD}$  Specification and Conditions<sup>1)2)</sup>

Parameter	Symbol	-7.5		Unit	Note/ Test Condition
		typ.	max.		
<b>Operating current</b> Single bank access cycles	$I_{DD1}$	—	65	mA	$t_{RC} = t_{RC,MIN}$ <sup>3)</sup>
<b>Precharge standby current</b> Power down mode	$I_{DD2P}$	—	0.6	mA	$\overline{CS} = V_{IH,MIN}$ , $CKE \leq V_{IL,MAX}$ <sup>3)</sup>
<b>Precharge standby current</b> Non power down mode	$I_{DD2N}$	—	20	mA	$\overline{CS} = V_{IH,MIN}$ , $CKE \geq V_{IH,MIN}$ <sup>3)</sup>
<b>Non operating current</b> Active state of 1 upto 4 banks, power down	$I_{DD3P}$	—	3.5	mA	$\overline{CS} = V_{IH,MIN}$ , $CKE \leq V_{IL,MAX}$ <sup>3)</sup>
<b>Non operating current</b> Active state of 1 upto 4 banks, non power down	$I_{DD3N}$	—	25	mA	$\overline{CS} = V_{IH,MIN}$ , $CKE \geq V_{IH,MIN}$ <sup>3)</sup>
<b>Burst operating current</b> Read command cycling	$I_{DD4}$	—	80	mA	<sup>3)4)</sup>
<b>Auto refresh current</b> Auto refresh command cycling	$I_{DD5}$	—	155	mA	$t_{RC} = t_{RC,MIN}$
<b>Self refresh current</b>	$I_{DD6}$	see <a href="#">Table 11</a>		$\mu A$	$t_{CK} = \text{infinity}$ , $CKE = 0.2 V$
<b>Deep power down mode current</b>	$I_{DD7}$	—	5	$\mu A$	

- 1)  $0\text{ }^{\circ}\text{C} \leq T_C \leq 70\text{ }^{\circ}\text{C}$  (comm.) and  $-25\text{ }^{\circ}\text{C} \leq T_{CASE} \leq +85\text{ }^{\circ}\text{C}$ ; recommended operating conditions unless otherwise noted
- 2) For proper power-up see the operation section of this data sheet.
- 3) These parameters depend on the frequency. These values are measured at 133MHz for -7.5 and at 100MHz for -8 parts. Input signals are changed once during  $t_{CK}$ . If the devices are operating at a frequency less than the maximum operation frequency, these current values are reduced.
- 4) These parameters are measured with continuous data stream during read access and all DQs toggling. CL = 3 and BL = 4 is used and the  $V_{DDQ}$  current is excluded.



**Table 11  $I_{DD6}$  Programmable Self Refresh Current<sup>1)2)</sup>**

Parameter	Symbol	-8	Unit	$T_{CASE}$	Note/ Test Condition
		max.		TCSR <sup>3)</sup>	
<b>Self refresh current</b> Self refresh mode, full array activations = all banks	$I_{DD6}$	t.b.d.	$\mu A$	max. 15°C	$t_{CK} = \text{infinity}$ , CKE = 0.2 V <sup>4)</sup>
		250	$\mu A$	max. 45°C	
		475	$\mu A$	max. 70°C	
		725	$\mu A$	max. 85°C	
<b>Self refresh current</b> Self refresh mode, half array activations = bank 0 + 1	$I_{DD6}$	t.b.d.	$\mu A$	max. 15°C	$t_{CK} = \text{infinity}$ , CKE = 0.2 V <sup>4)</sup>
		150	$\mu A$	max. 45°C	
		250	$\mu A$	max. 70°C	
		450	$\mu A$	max. 85°C	
<b>Self refresh current</b> Self refresh mode, quarter array activations = bank 0	$I_{DD6}$	t.b.d.	$\mu A$	max. 15°C	$t_{CK} = \text{infinity}$ , CKE = 0.2 V <sup>4)</sup>
		100	$\mu A$	max. 45°C	
		150	$\mu A$	max. 70°C	
		275	$\mu A$	max. 85°C	

- 1) Recommended operating conditions unless otherwise noted.
- 2) For proper power-up see the operation section of this data sheet.
- 3) Extended Mode Register A4-A3.
- 4) Target values to be verified on final product and may change.



## 5 Package Outline

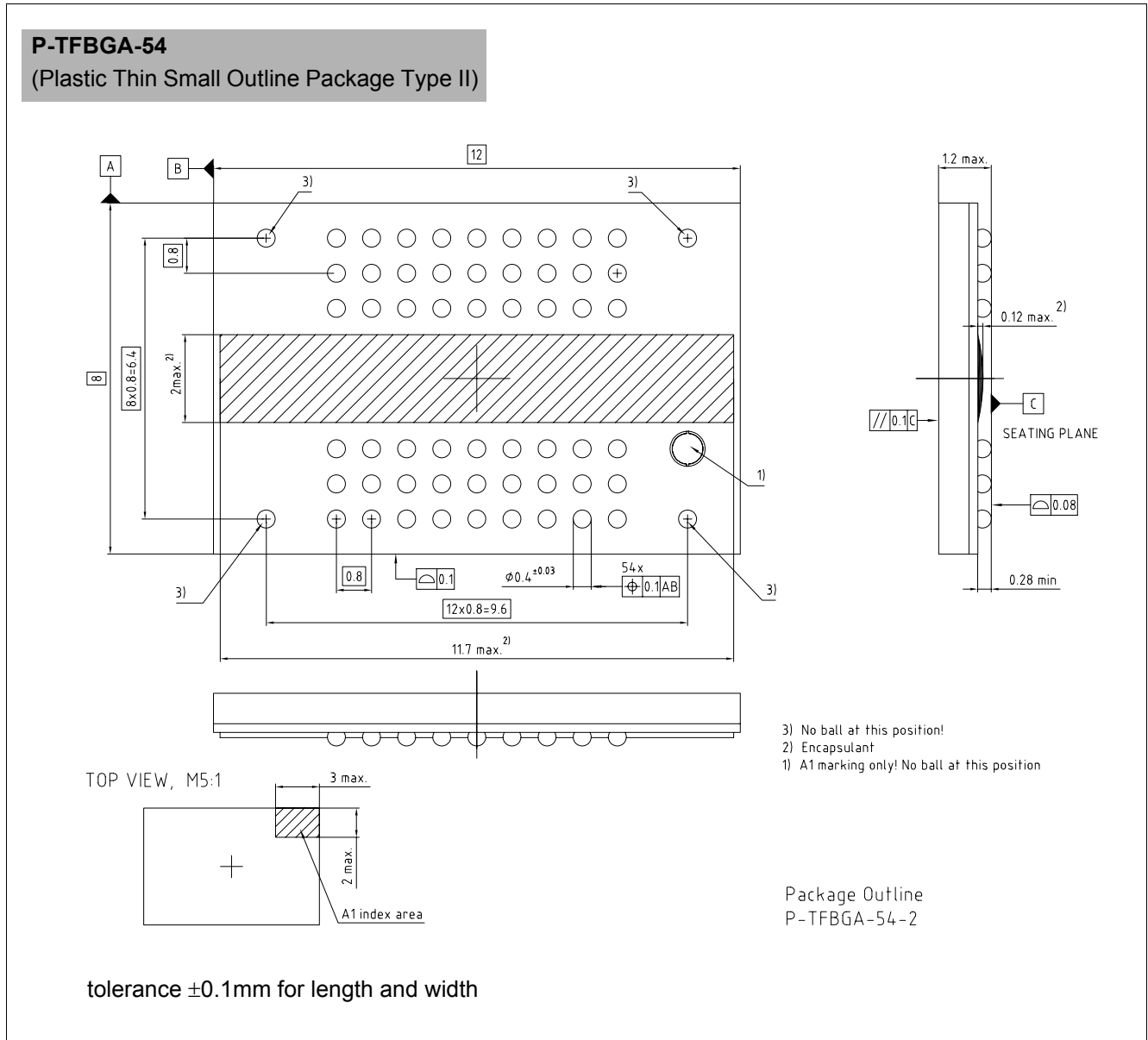


Figure 3 Package Outline

You can find all of our packages, sorts of packing and others in our Qimonda Internet Page:

<http://www.qimonda.com>.

SMD = Surface Mounted Device

Dimensions in mm





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